REMARKS

In the present Office Action, claims 33-113 were examined. Claims 33-37, 52-62, 91-97, 112 and 113 were rejected by the Examiner. Claims 38-51, 63-90 and 98-111 were objected to and no claims were allowed.

By this Response no claims have been amended, no claims have been canceled, and no claims have been added. Accordingly, claims 33 to 113 are presented for further examination. No new matter has been added. By this Amendment, claims 33-113 are believed to be in condition for allowance.

Explanation of Above Amendments

In the present office action, the Examiner rejected claims 33 to 27 and 93 to 97 under 35 U.S.C. §102(e) as being anticipated by Maehara et al. (U.S. Patent No. 6,075,715). In making this rejection, the Examiner stated the following:

> "Regarding claims 33-35, 93-95, Maehara et al. (Fig. 30) disclose an electrical circuit comprising: a power source (1); elements (C3, La, T1) can be broadly reads as a load; a switching bridge (Q1,Q2); a bridge capacitor (C1), diodes (D1, D2), wherein the connections between these elements are inherently disclosed.
>
> Regarding claims 36, 37, 96, 97, wherein switches are bipolar transistors."

As previously mentioned in the Response dated January 7, 2004, to an earlier Office Action, wherein the Examiner made a similar rejection under 35 U.S.C. §103(b), Maehara et al. differs from the present claims in many ways.

There are huge differences in the principle of the operation between circuits described in Maehara et al. and the boost bridge amplifier of claims 33-37 and the boost bridge amplifier of claims 93-97. For example, one resonant circuit of Maehara et al. is formed from the load circuitry (3) reflected to primary of the transformer T1, primary of the transformer T1 and the second capacitor C2 of small value, through switch Q2 and diode D2, or through the first capacitor C1, switch Q1 and diode D1. (See claim 1 of the reference.)

Another resonant circuit of Maehara et al. is formed from the load circuitry (3), the inductance circuit and the second capacitor C2 of small value, through switch Q2 and diode D2, or through the first capacitor C1, switch Q1 and diode D1. (See claim 2.)

Furthermore, Fig. 7 and Fig. 8 of Maehara et al. disclose timing diagrams with extremely variable capacitor C2 voltage VC2, due to the operation in resonance.

In contrast, Figs. 11, 14, 17 and 20 of the present specifications and appropriate claims 33, 34, 35, 93, 94 and 95 of the present invention are directed to circuit of load 5 comprising resistance and smoothing inductance connected in series.

In addition, the power supply 1 of the present invention is a DC power supply with constant voltage which is contrary to extremely variable capacitor C2 voltage VC2, used in Maehara et al..

Therefore, it is quite clear that the operation of claimed boost bridge amplifier of the present invention is free from any resonances utilized in Maehara et al. It should be noted that the ordinary skilled artisan in this field of power electronics would clearly recognize the differences between resonant (as illustrated by Maehara et al.) and non-resonant converters (such as the present invention). This demarcation is shown in the following book: Ned Mohan, Tore M. Undeland, William P. Robbins; "Power Electronics: Converters, Applications and Design"; 3rd Edition, John Wiley and Sons, October 2002. Note that this book has separate chapters directed to these two different types of converters (see Chapters 8 and 9).

Stated another way, independent claims 33 and 93 of the present application utilize less number of elements to operate than Maehara et al. Furthermore, neither one of circuits disclosed in Maehara et al. will operate with DC power source (1) alone, since all of them require an additional element: the capacitor C2 of small value. Therefore, claims 33-37, 93-97 are not anticipated by Maehara et al., and are patentable together with claims 112 and 113 are patentable.

Rejections under 35 USC §103

The Examiner rejected claim 52-62, 91, 92 and 113 under 35 U.S.C. §103(a) as being obvious and unpatentable in view of Maehara et al. In making this obviousness rejection, the Examiner stated the following:

> "Regarding claims 52, 53, 91, 92, 112, 113, Maehara et al. disclose the claimed invention except the specific load as claimed. However, such as load would have been considered a matter of design choice in the absence of unexpected results if not an intended use of the invention, wherein Maehara et al. disclose a specific load as discharge lamp. Regarding claims 54-56, 58, 59, Maehara et al. disclose the claimed invention an output filter having the connection thereof. Maehara et al. (Fig. 30) disclose a electrical circuit comprising: a power source (1); a load (C3, La, T1); a switching bridge (Q1, Q2); a bridge capacitor (C1); a filtering capacitor (C4); diodes (D1, D2), wherein the connections between these elements are inherently disclosed. However, it is known in the art that addition of a known type filter will only enhance circuit operation, such as filtering out noise or improving output signal. As such, adding a filter to a circuit would have been considered a matter of design choice/engineering.
>
> Regarding claims 57, 60-62, wherein switches are bipolar transistors."

Applicant respectfully traverses this rejection for the following reasons.

Please find attached with this response slides accompanying the Chapter 19 Resonant Conversion prepared by Prof. Dr. R. W. Erickson from his famous book, "Fundamentals of Power Electronics", teaching the specifics of the operation of resonant power converters (used in Maehara et al.), as well as Chapter 6 Converter Circuits from the same source, teaching the operation of non-resonant converters (used in this patent application).

It is obvious that there is not a single one schematic of non-resonant converters in Chapter 6 having a resonant capacitor in parallel with the power source, while ALL parallel resonant converters in Chapter 19 have a resonant capacitor (like C2 in Maehara et al.) in parallel with diode bridge.

Since Maehara et al. requires at least one additional element to operate and has completely different operating principle in comparison with our invention, this difference alone should be sufficient to grant this U.S. Patent.

First, the arguments made in response to previous rejection are also applicable here.

Present claims 52, 91 and 113 are limited to a dual voice coil loudspeaker as load (5). This type of load provides special effects on the power supply (1) current and generated average force, disclosed in the description (see page 11, lines 1 to 17 of underlying PCT Appl. WO01/01554). Since these effects cannot be provided by Maehara et al., claims 52, 91 and 112 should not be rejected as being obvious over its teachings for this reason alone.

Present claims 53, 92 and 113 also are limited to three-phase electric motor as load (5). This type of load provides special effects on power supply (1) current and generated average force, disclosed in the description (see page 12, lines 17 to 31, and page 13, lines 1 to 3 of WO01/01554). Since these effects cannot be provided by Maehara et al., claims 53, 92 and 113 should not be rejected as being obvious.

Present claims 36, 37, 57, 60, 61, 62, 96 and 97 circuits described in claims 35, 34, 56, 59, 58, 55, 95 and 94, are further limited utilization of semiconductor switches as active switches. Since claims 36, 37, 57, 60, 61, 62, 96 and 97 are dependent upon, respectively, and those dependent claims incorporate those unobvious features that should not be rejected.

In the first paragraph of the present Office Action, the Examiner commented that Applicant had previously argued that "load (5) is **directly coupled** with the power supply (1) allowing DC current through load (5) for supplying switching bridge (3)", but argued that claims 33, 54 and 93 are so limited. The Examiners comments have been considered, but it is believed that the claim language in these claims "the first node of said power supply (1) is connected to the first node of each phase of said load (5)" is proper. While the language in the specification referring to Fig. 2 talks about directly connecting the load (5) to the power supply (1), there are other embodiments that talk about the inclusion of other structures (e.g. an input filter) between the power supply and the load.

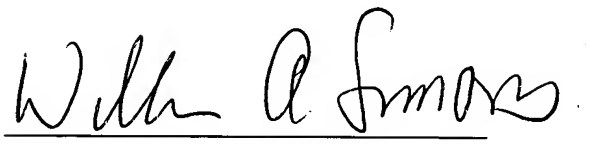
Applicant is pleased to see that claims 38-51, 63-90 and 98-111 are allowable. At the present time, for cost considerations, Applicant will not make claims 38, 63 and 98 into independent claims at this time.

Accordingly, Applicant submits that the cites referenced, does not anticipate or make obvious the invention as presently claimed and that the application is now in condition for allowance. Therefore, Applicant respectfully requests reconsideration and further examination of the application and the Examiner is respectfully requested to take such proper actions so that a patent will issue herefrom as soon as possible.

If the Examiner has any questions or believes that a discussion with Applicant's attorney would expedite prosecution, the Examiner is invited and encouraged to contact the undersigned at the telephone number below.

Please apply any credits or charge any deficiencies to our Deposit Account No. 23-1665.

Respectfully submitted,
M. Prokin et al.



William A. Simons, Reg. No. 27,096

January 31, 2005

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APPENDIX:

Dr. R. W. Erickson, "Fundamentals of Power Electronics", Chapter 6, Converter Circuits, 100pp.

Dr. R. W. Erickson, "Fundamentals of Power Electronics", Chapter 19, Resonant Conversion, 87pp.

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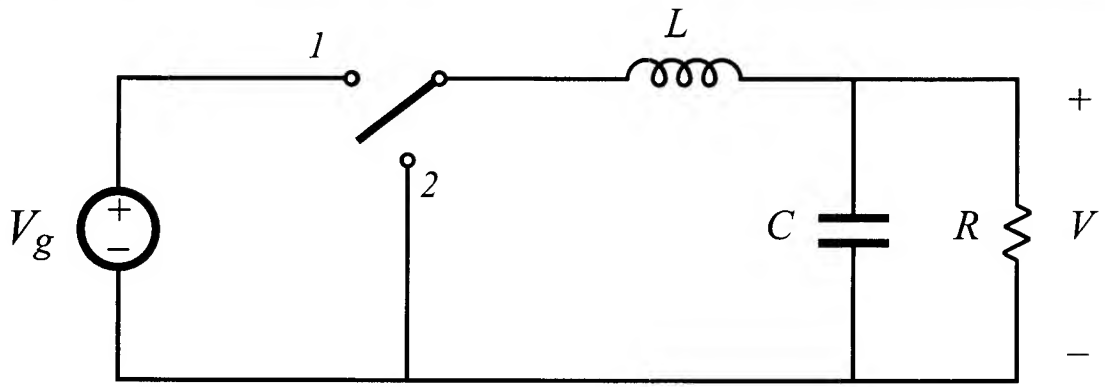
Chapter 6. Converter Circuits

- Where do the boost, buck-boost, and other converters originate?
- How can we obtain a converter having given desired properties?
- What converters are possible?
- How can we obtain transformer isolation in a converter?
- For a given application, which converter is best?

6.1. Circuit manipulations



Begin with buck converter: derived in chapter 1 from first principles

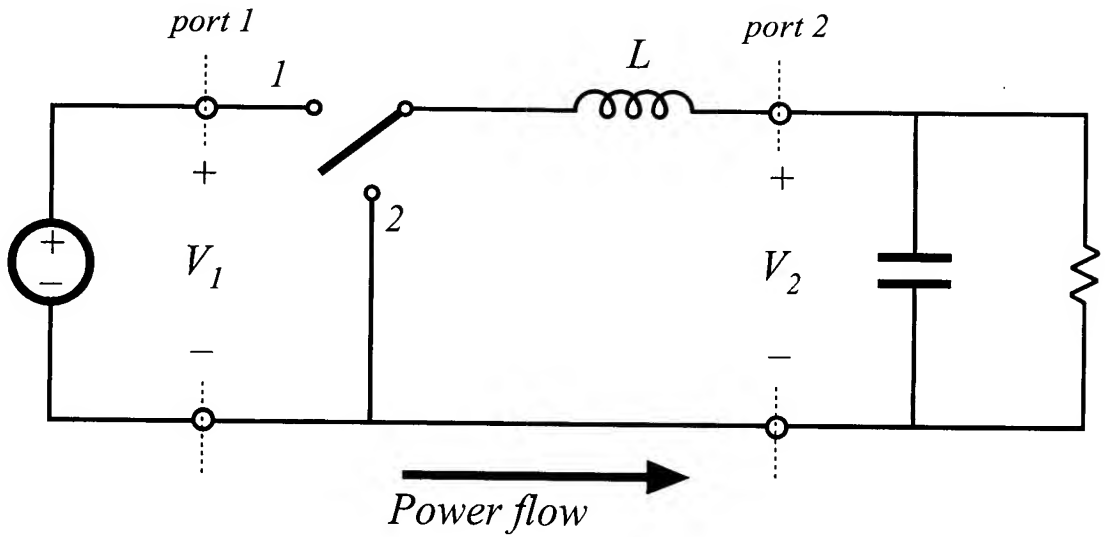
- Switch changes dc component, low-pass filter removes switching harmonics
- Conversion ratio is $M = D$

6.1.1. Inversion of source and load

Interchange power input and output ports of a converter

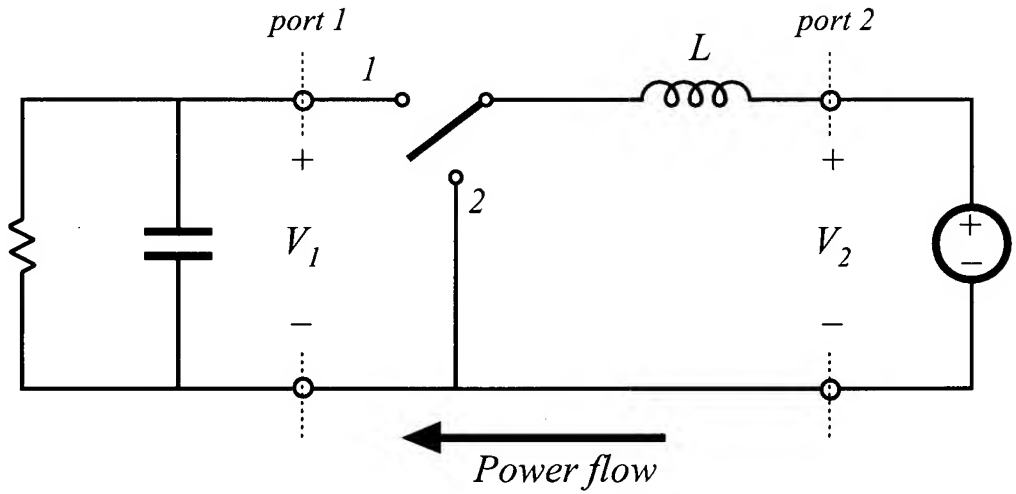
Buck converter example

$$V_2 = DV_1$$



Inversion of source and load

Interchange power source and load:

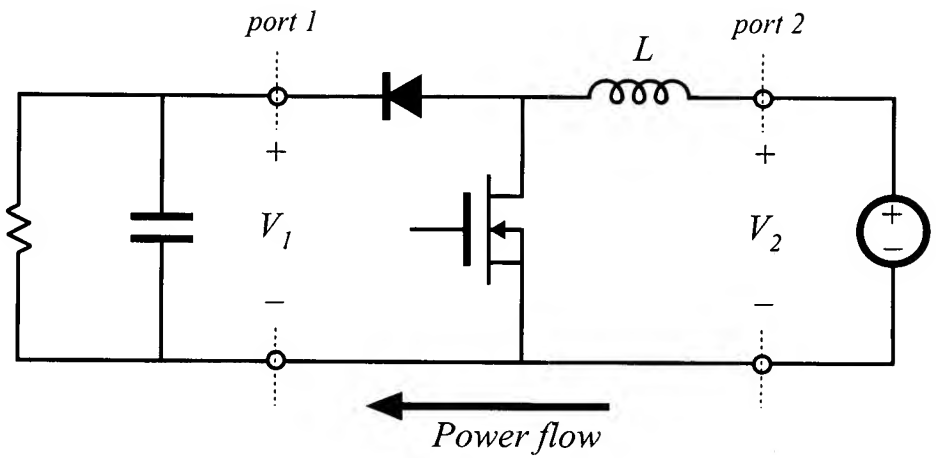


$$V_2 = DV_1 \qquad V_1 = \frac{1}{D} V_2$$

Realization of switches as in chapter 4

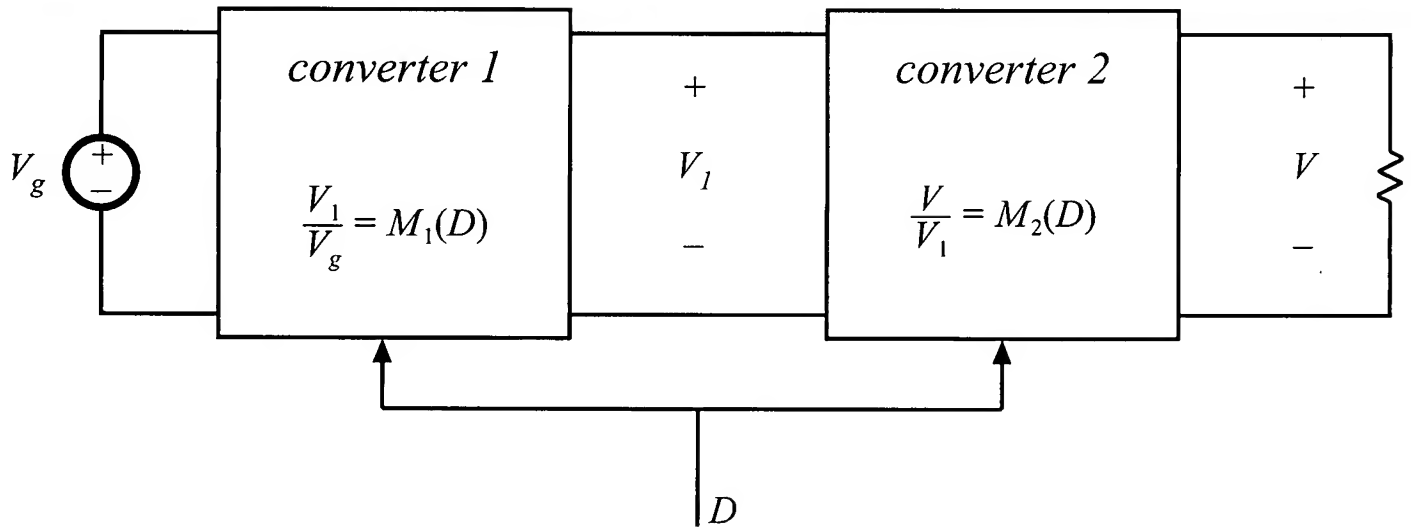
- Reversal of power flow requires new realization of switches
- Transistor conducts when switch is in position 2
- Interchange of D and D'

$$V_1 = \frac{1}{D'} V_2$$



Inversion of buck converter yields boost converter

6.1.2. Cascade connection of converters

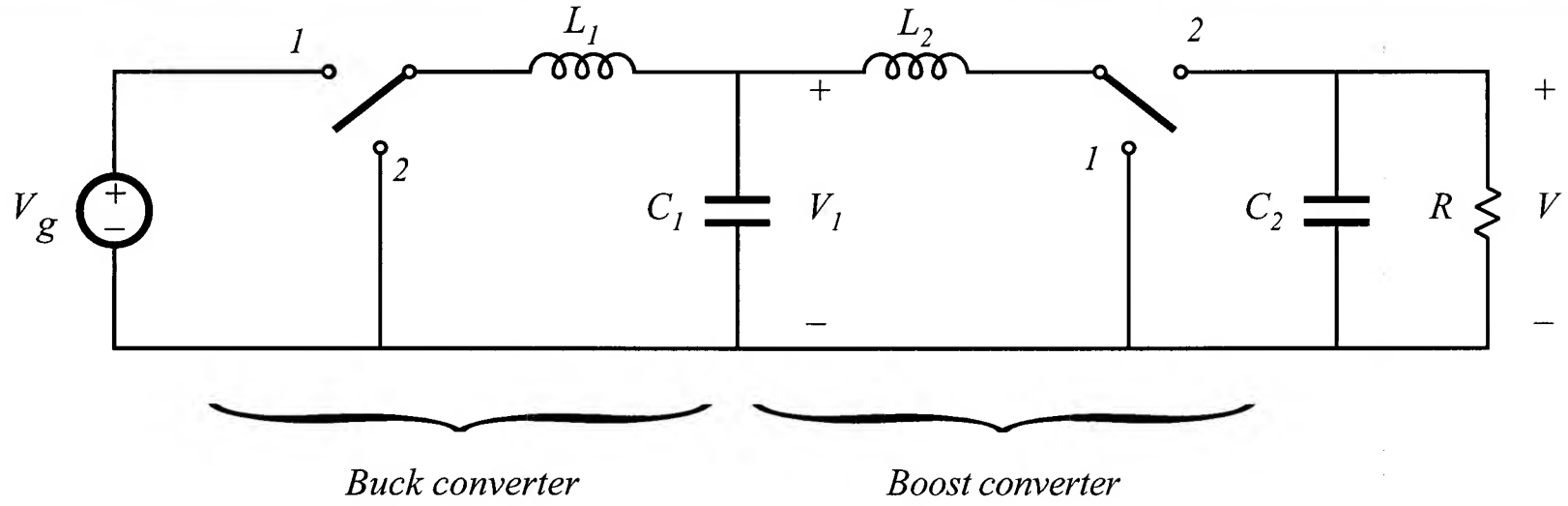


$$V_1 = M_1(D)\, V_g$$

$$V = M_2(D)\, V_1$$

$$\rightarrow \quad \frac{V}{V_g} = M(D) = M_1(D)\, M_2(D)$$

Example: buck cascaded by boost



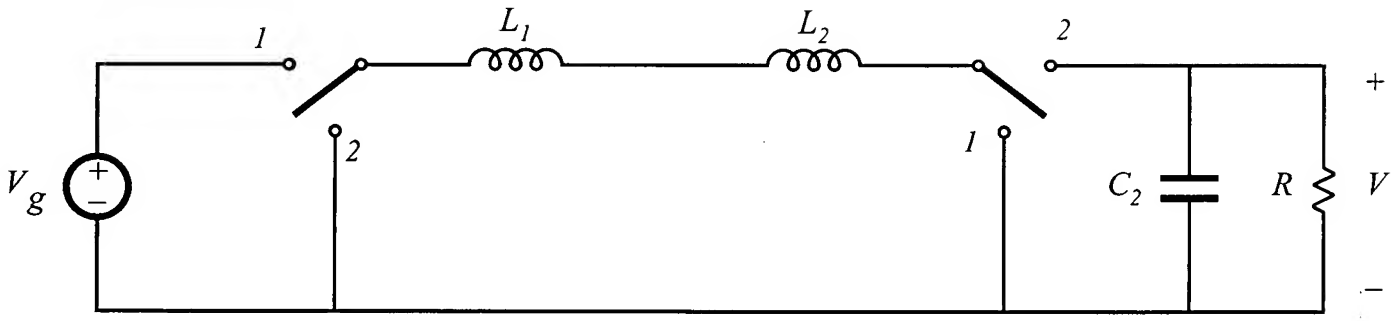
$$\frac{V_1}{V_g} = D$$

$$\frac{V}{V_1} = \frac{1}{1-D}$$

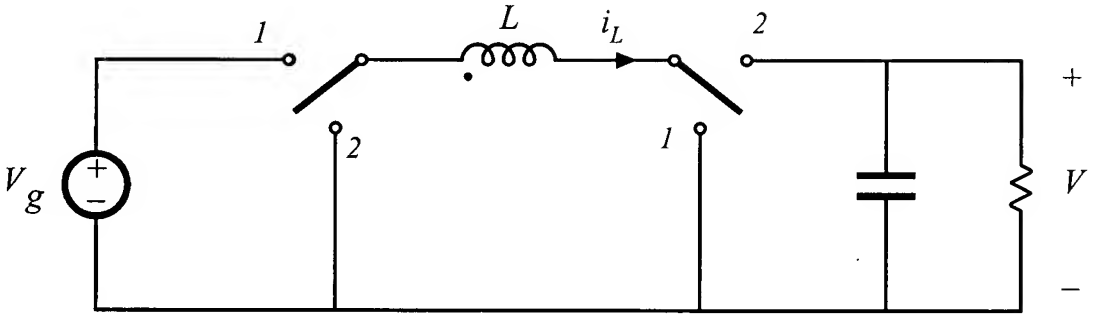
$$\rightarrow \quad \frac{V}{V_g} = \frac{D}{1-D}$$

Buck cascaded by boost: simplification of internal filter

remove capacitor C_1

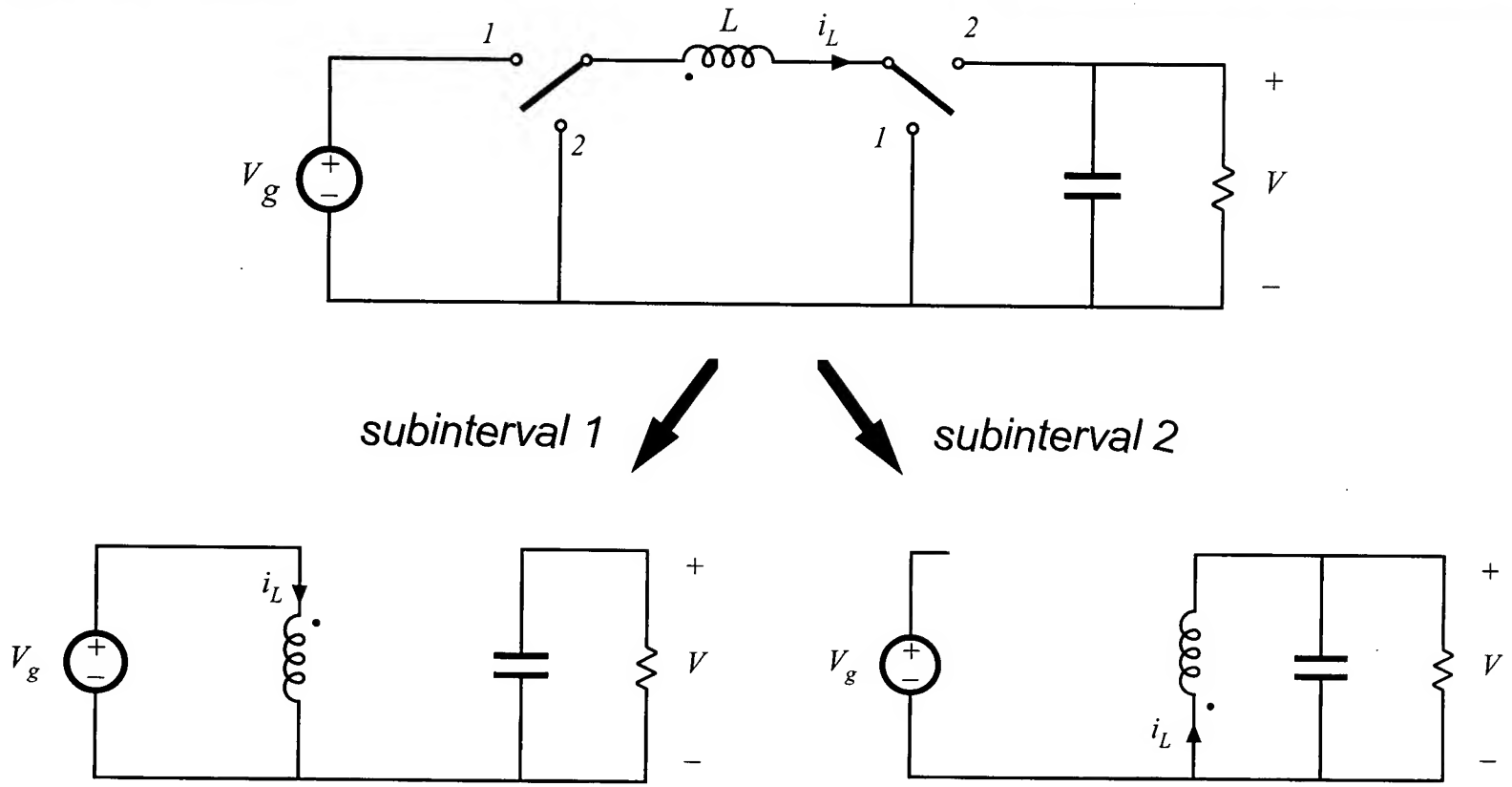


combine inductors L_1 and L_2

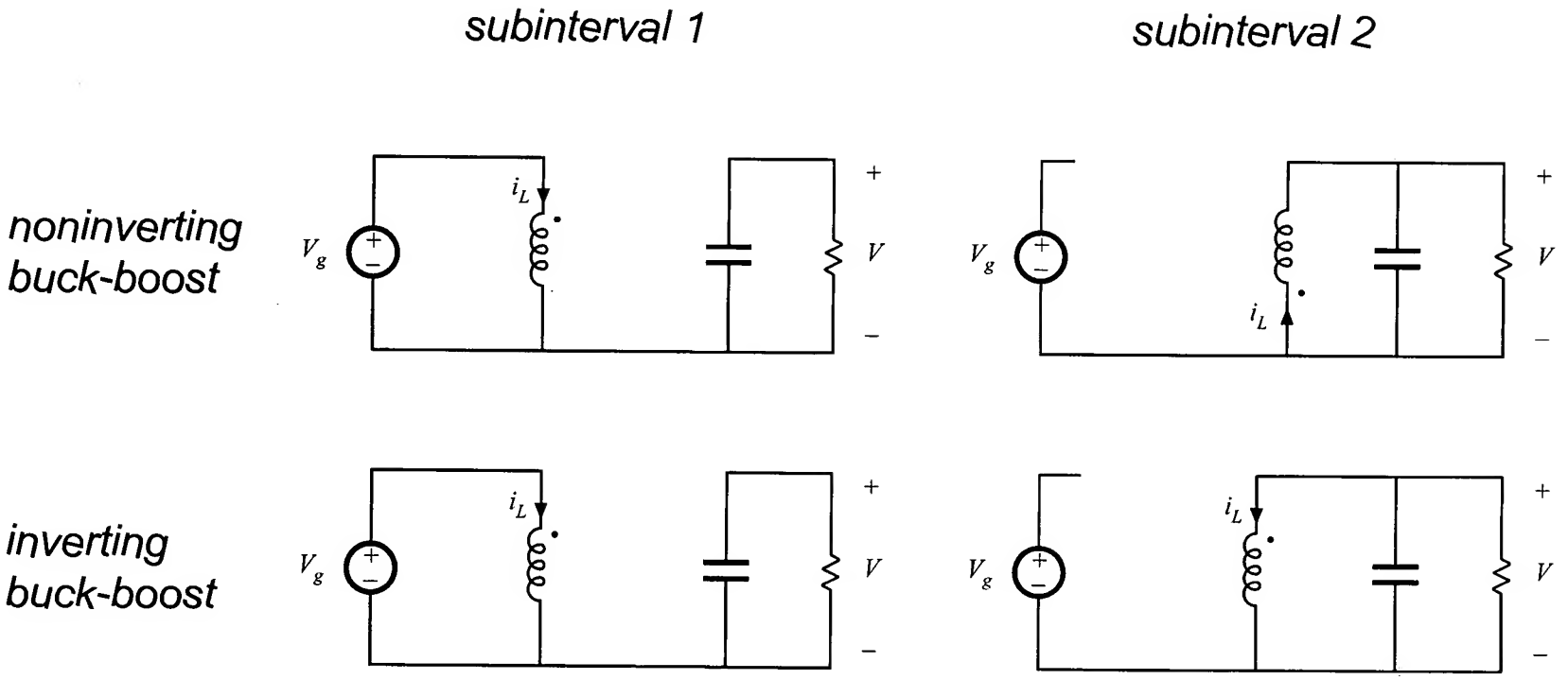


Noninverting buck-boost converter

Noninverting buck-boost converter

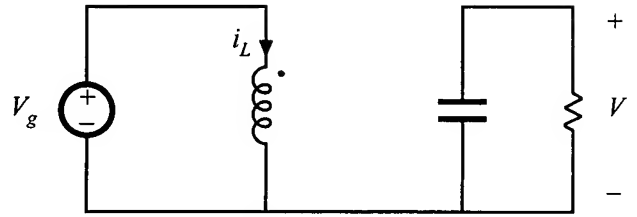


Reversal of output voltage polarity

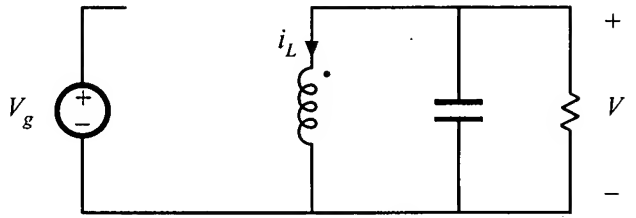


Reduction of number of switches: inverting buck-boost

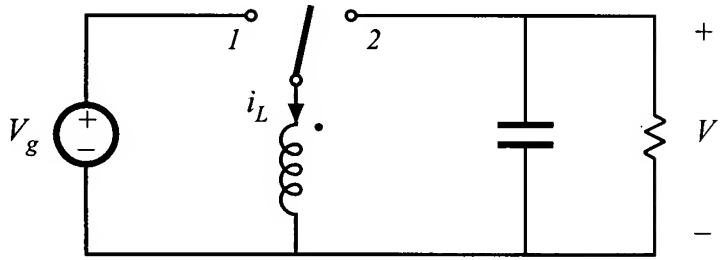
subinterval 1



subinterval 2



One side of inductor always connected to ground — hence, only one SPDT switch needed:



$$\frac{V}{V_g} = -\frac{D}{1-D}$$

Discussion: cascade connections

- Properties of buck-boost converter follow from its derivation as buck cascaded by boost

  Equivalent circuit model: buck 1:D transformer cascaded by boost D':1 transformer

  Pulsating input current of buck converter

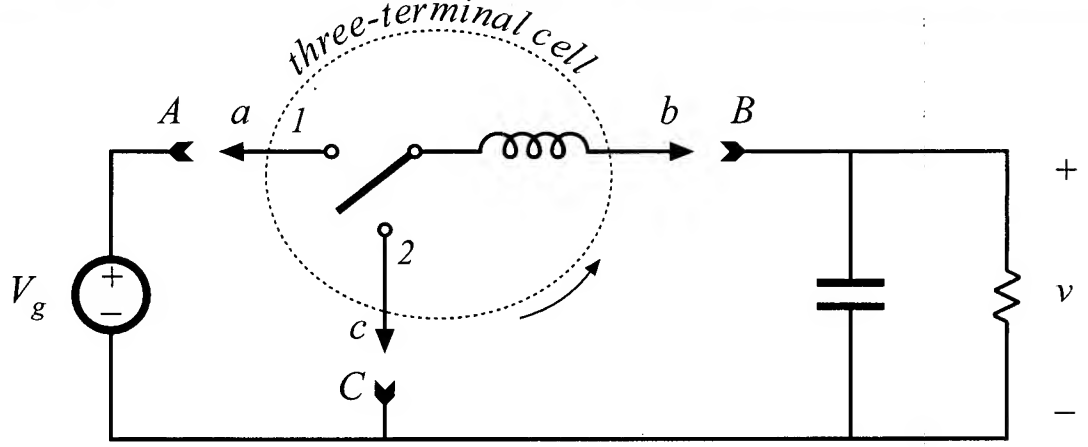
  Pulsating output current of boost converter

- Other cascade connections are possible

  Cuk converter: boost cascaded by buck

6.1.3. Rotation of three-terminal cell

Treat inductor and SPDT switch as three-terminal cell:

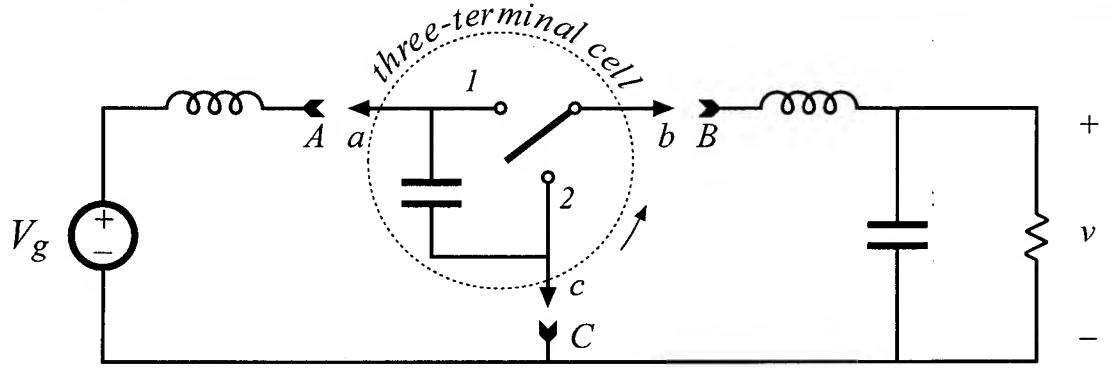


Three-terminal cell can be connected between source and load in three nontrivial distinct ways:

a-A b-B c-C	buck converter
a-C b-A c-B	boost converter
a-A b-C c-B	buck-boost converter

Rotation of a dual three-terminal network

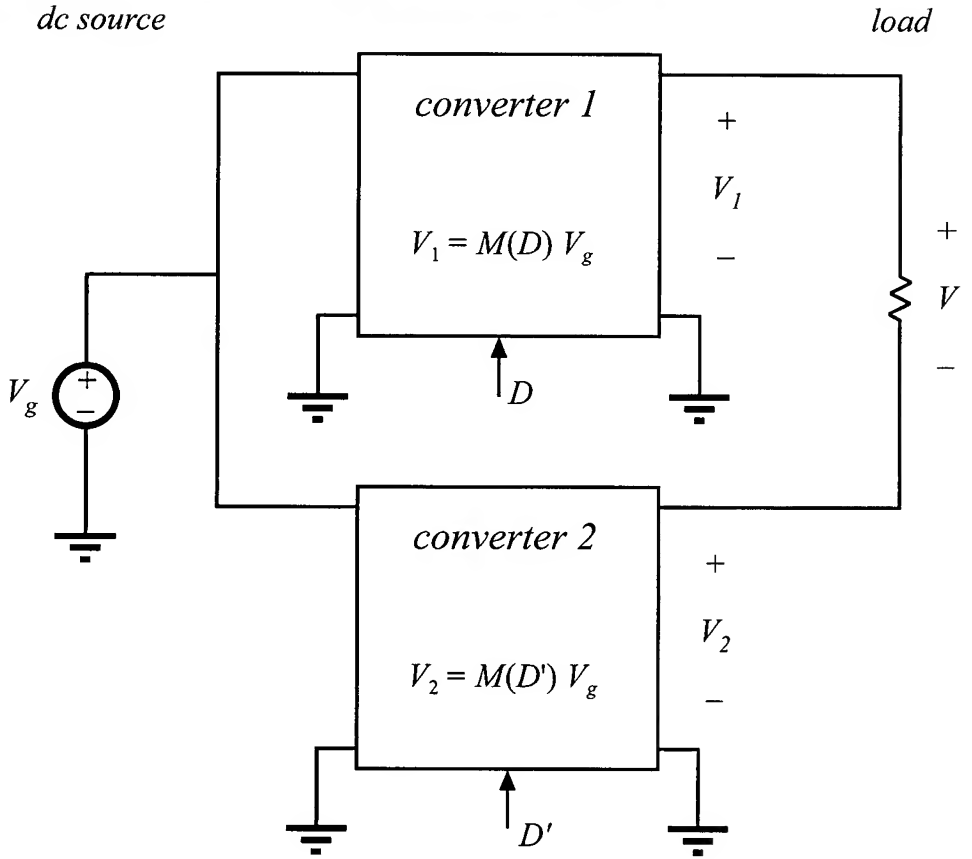
A capacitor and SPDT switch as a three-terminal cell:



Three-terminal cell can be connected between source and load in three nontrivial distinct ways:

a-A b-B c-C	buck converter with L-C input filter
a-C b-A c-B	boost converter with L-C output filter
a-A b-C c-B	Cuk converter

6.1.4. Differential connection of load to obtain bipolar output voltage

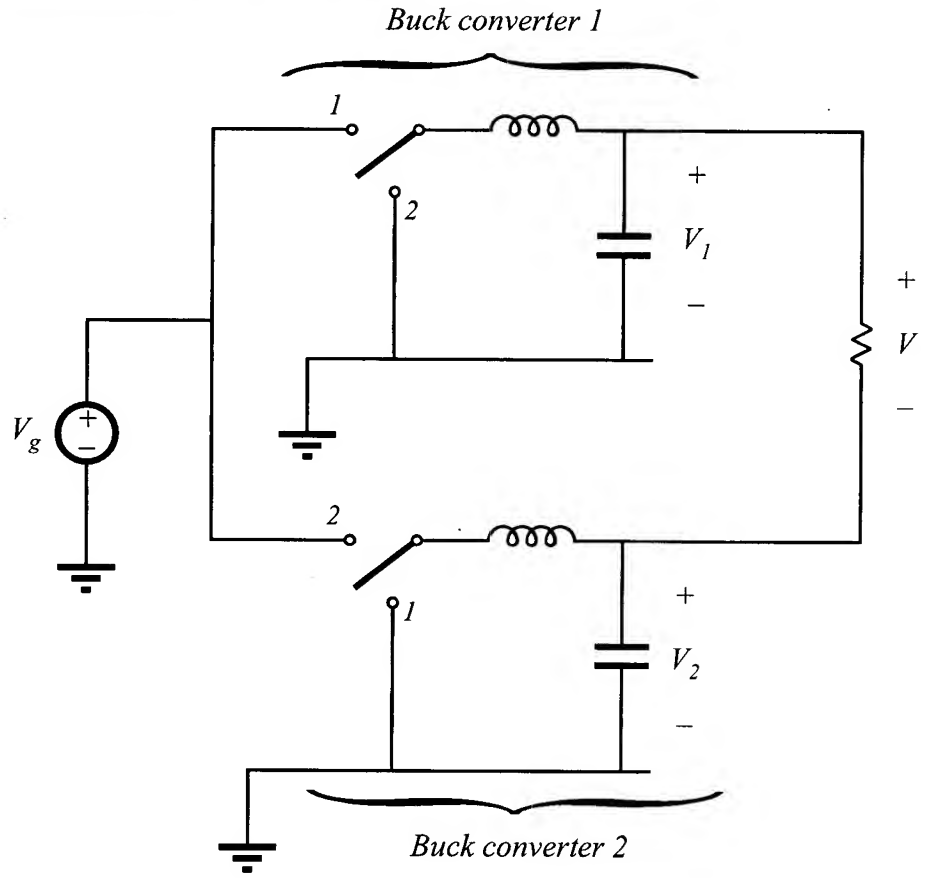


Differential load voltage is

$$V = V_1 - V_2$$

The outputs V_1 and V_2 may both be positive, but the differential output voltage V can be positive or negative.

Differential connection using two buck converters



Converter #1 transistor driven with duty cycle D

Converter #2 transistor driven with duty cycle complement D'

Differential load voltage is

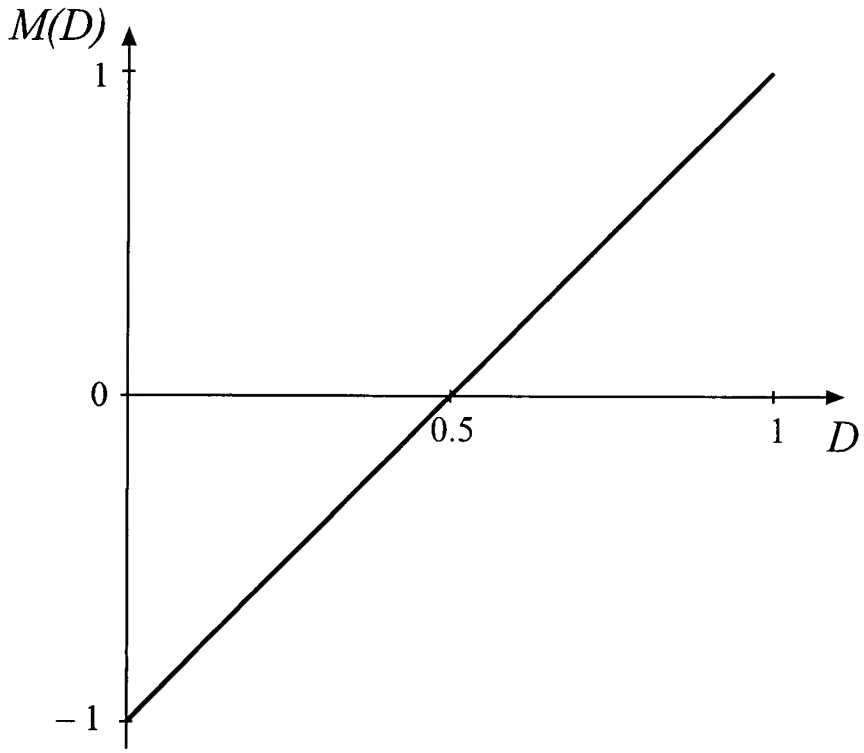
$$V = DV_g - D'V_g$$

Simplify:

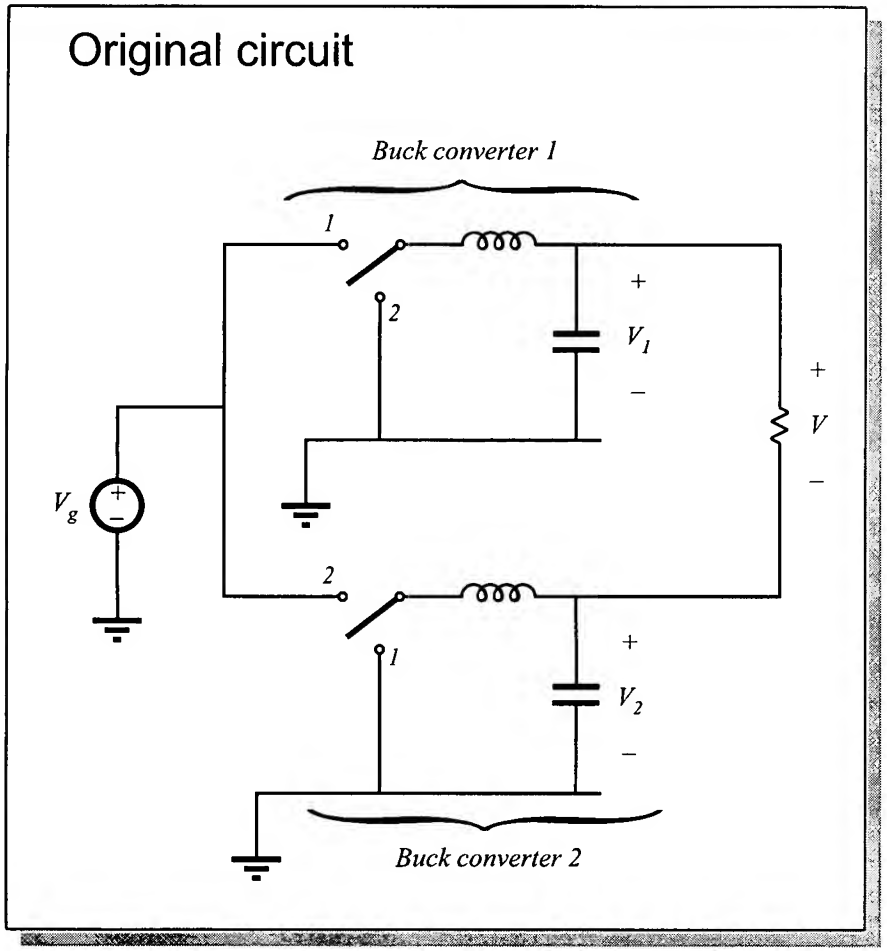
$$V = (2D - 1)\, V_g$$

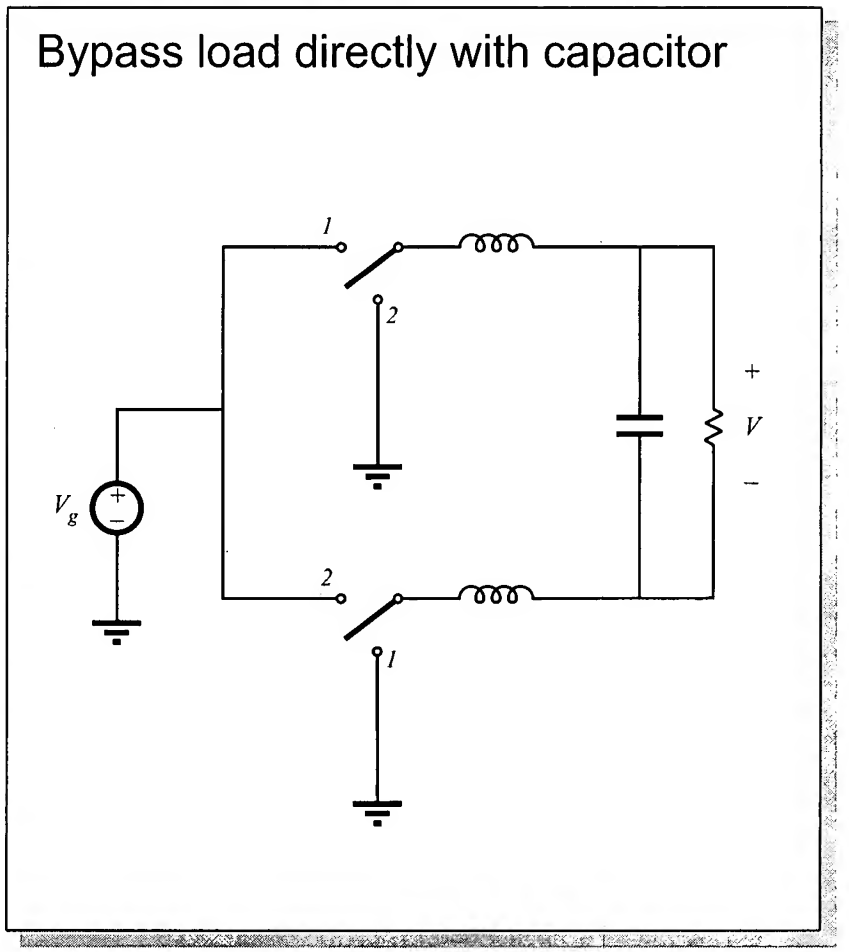
Conversion ratio *M(D)*, differentially-connected buck converters

$$V = (2D - 1)\, V_g$$



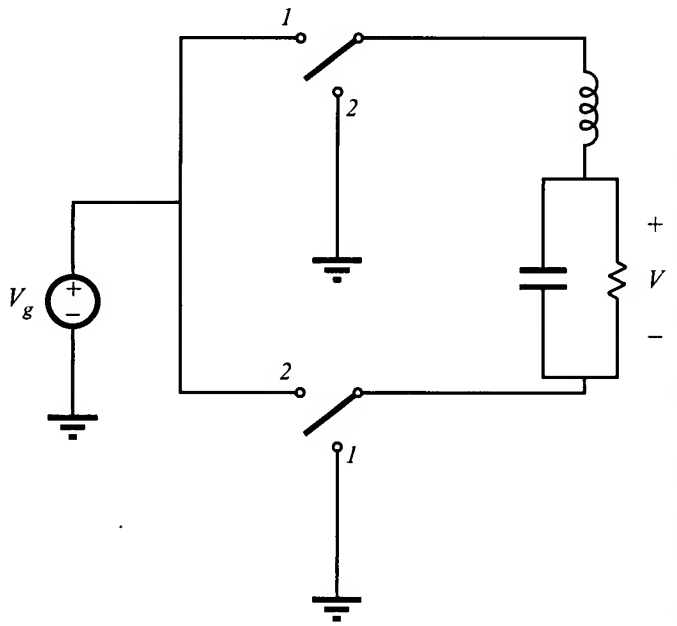
Simplification of filter circuit, differentially-connected buck converters



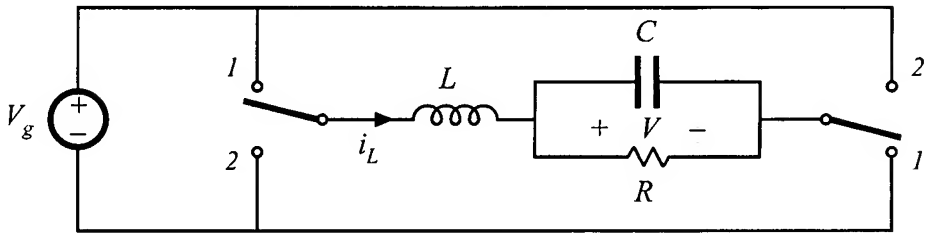


Simplification of filter circuit, differentially-connected buck converters

Combine series-connected inductors



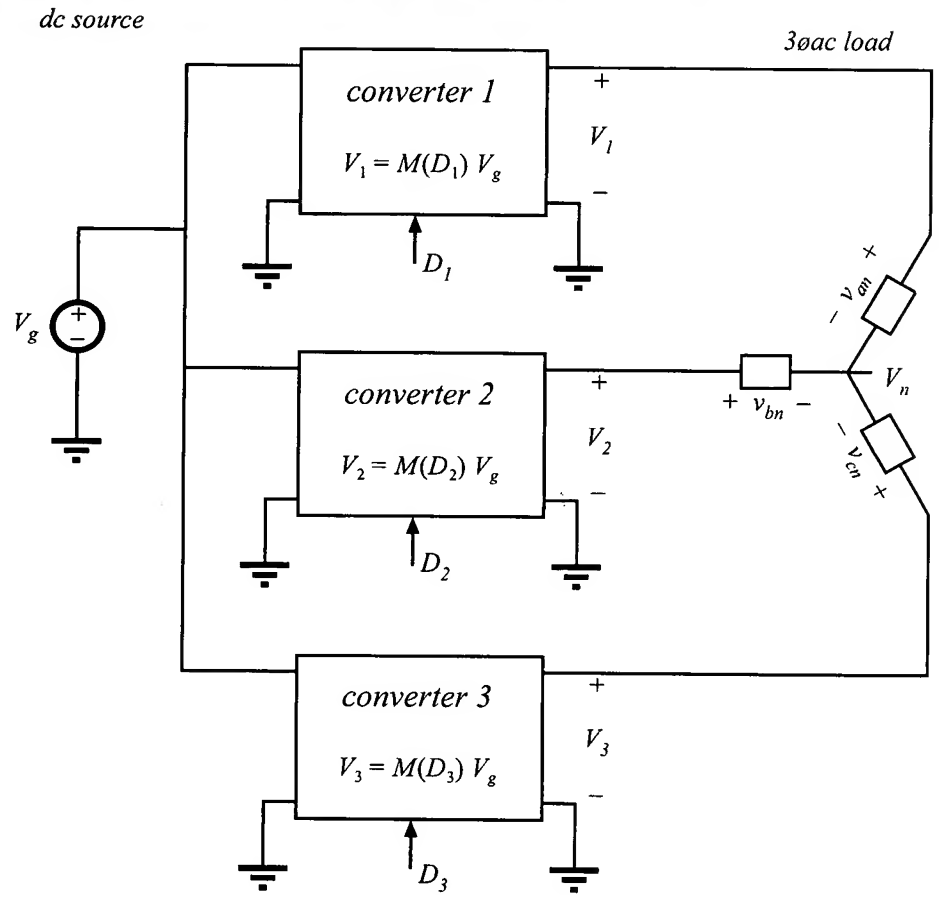
Re-draw for clarity



H-bridge, or bridge inverter

Commonly used in single-phase inverter applications and in servo amplifier applications

Differential connection to obtain 3ø inverter



With balanced 3ø load, neutral voltage is

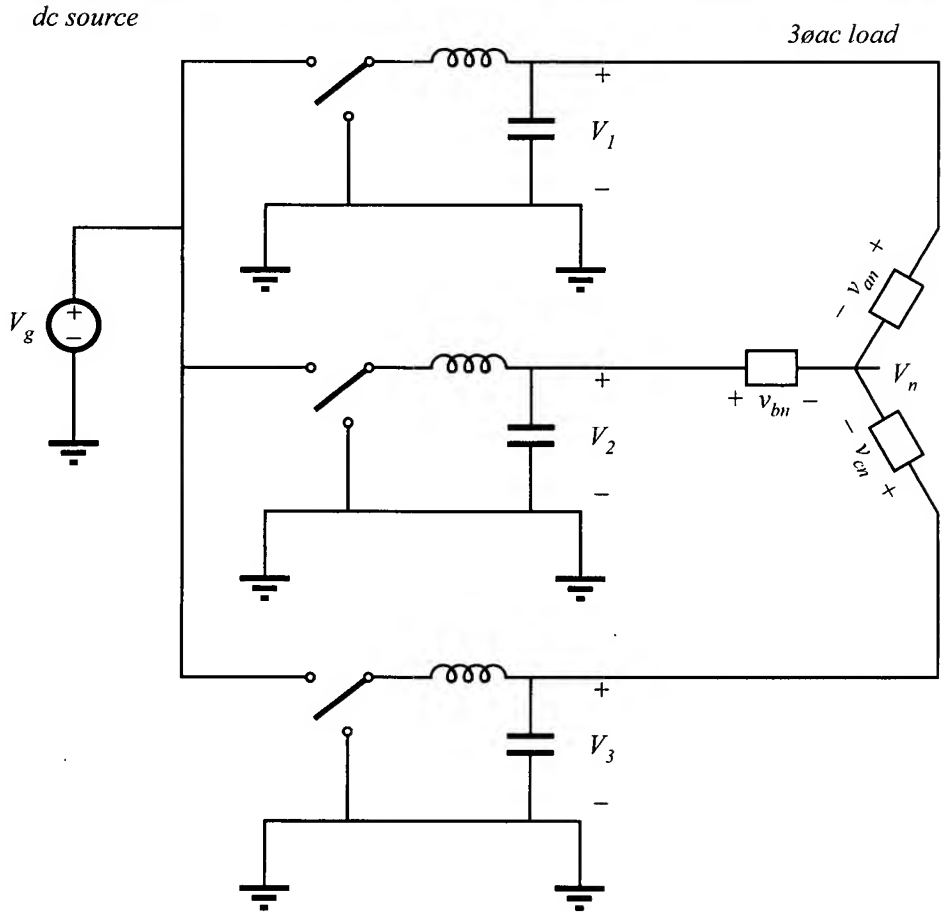
$$V_n = \frac{1}{3}(V_1 + V_2 + V_3)$$

Phase voltages are

$$V_{an} = V_1 - V_n$$
$$V_{bn} = V_2 - V_n$$
$$V_{cn} = V_3 - V_n$$

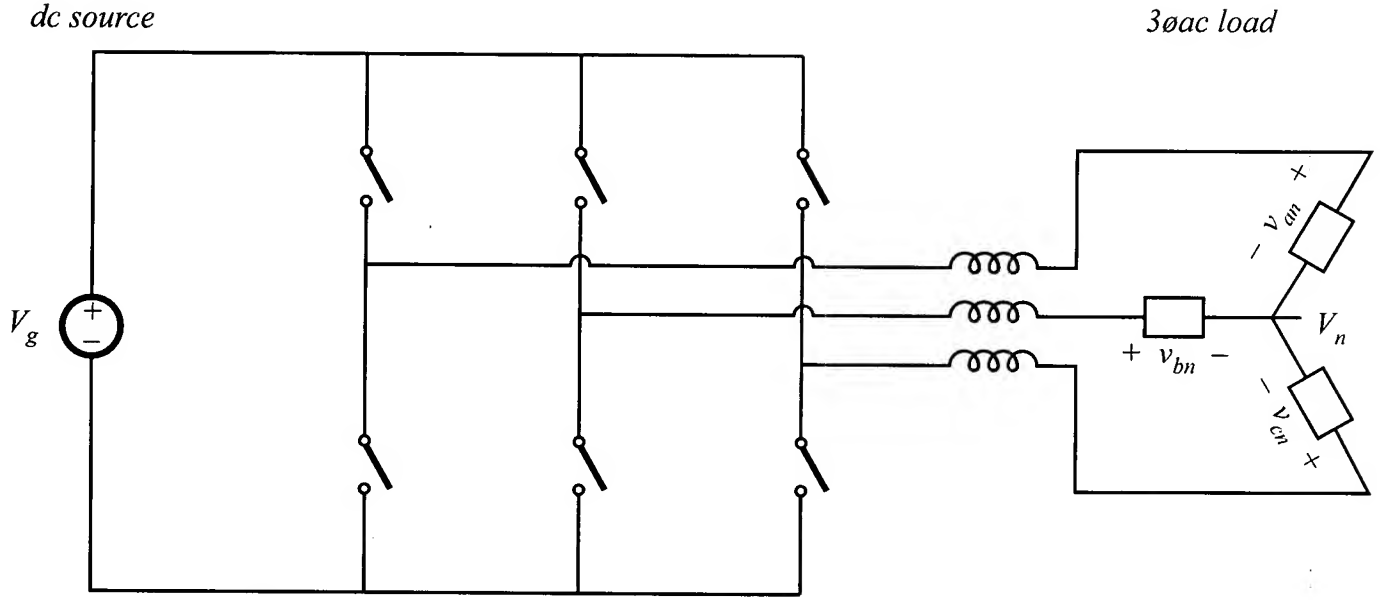
Control converters such that their output voltages contain the same dc biases. This dc bias will appear at the neutral point Vn. It then cancels out, so phase voltages contain no dc bias.

3ø differential connection of three buck converters



3ø differential connection of three buck converters

Re-draw for clarity:



"Voltage-source inverter" or buck-derived three-phase inverter

6.2. A short list of converters

An infinite number of converters are possible, which contain switches embedded in a network of inductors and capacitors

Two simple classes of converters are listed here:

- Single-input single-output converters containing a single inductor. The switching period is divided into two subintervals. This class contains eight converters.
- Single-input single-output converters containing two inductors. The switching period is divided into two subintervals. Several of the more interesting members of this class are listed.

Single-input single-output converters containing one inductor

- Use switches to connect inductor between source and load, in one manner during first subinterval and in another during second subinterval
- There are a limited number of ways to do this, so all possible combinations can be found
- After elimination of degenerate and redundant cases, eight converters are found:

dc-dc converters

buck boost buck-boost noninverting buck-boost

dc-ac converters

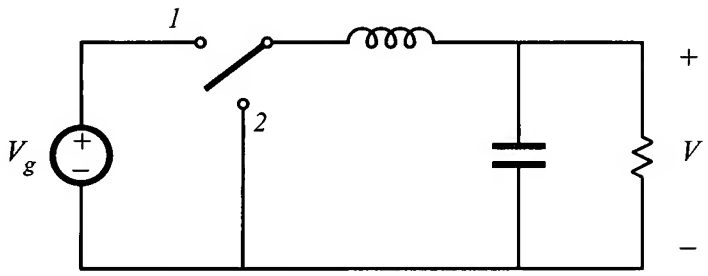
bridge Watkins-Johnson

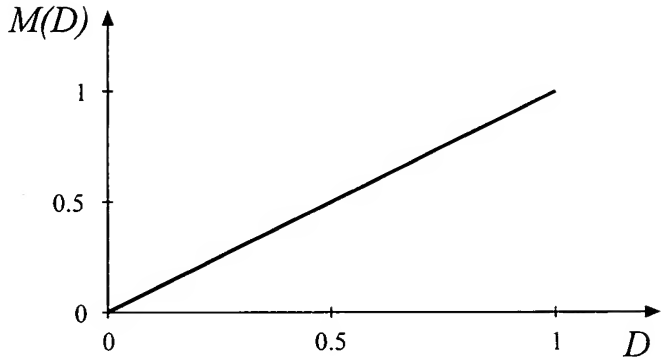
ac-dc converters

current-fed bridge inverse of Watkins-Johnson

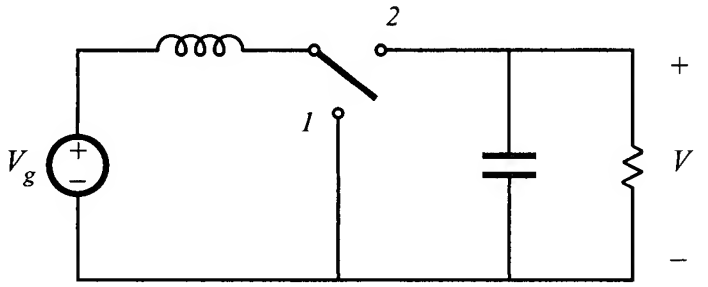
Converters producing a unipolar output voltage

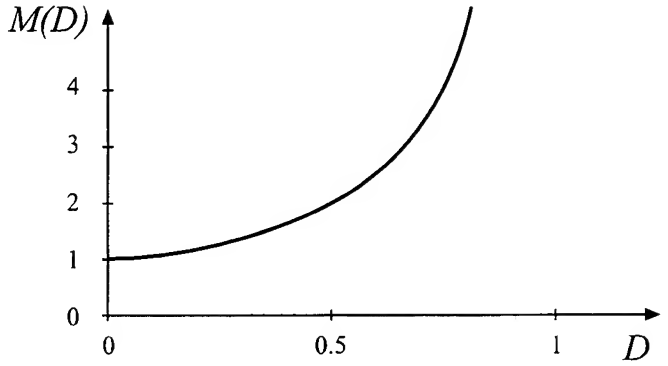
1. *Buck* $M(D) = D$





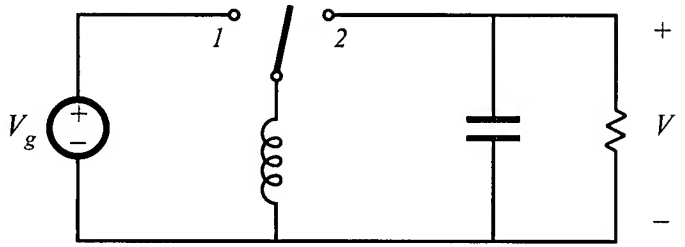
2. *Boost* $M(D) = \frac{1}{1-D}$

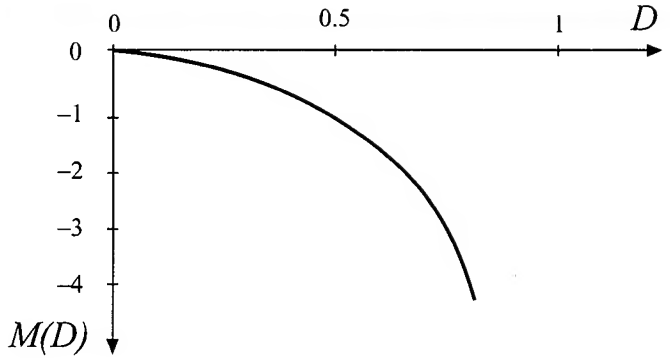




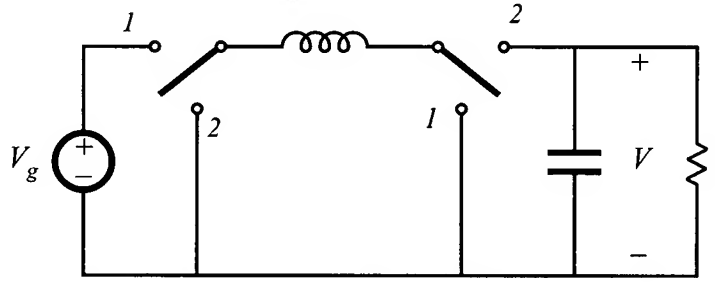
Converters producing a unipolar output voltage

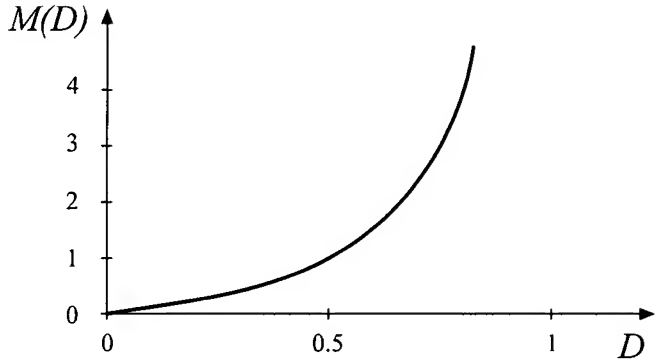
3. *Buck-boost* $M(D) = -\frac{D}{1-D}$





4. *Noninverting buck-boost* $M(D) = \frac{D}{1-D}$

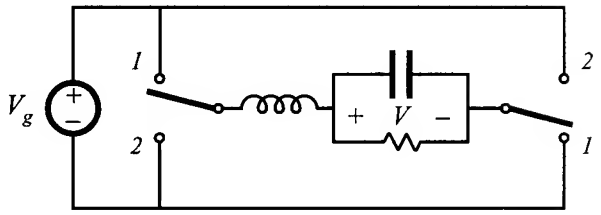


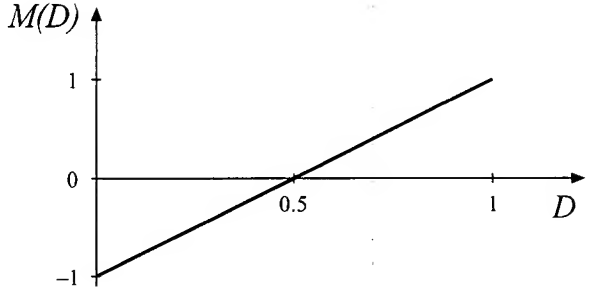


Converters producing a bipolar output voltage suitable as dc-ac inverters

5. *Bridge*

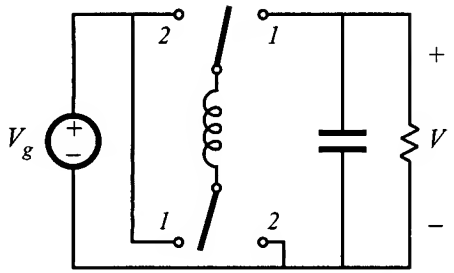
$M(D) = 2D - 1$



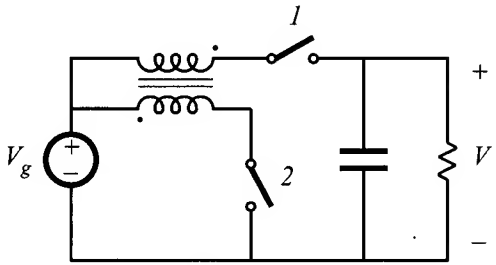


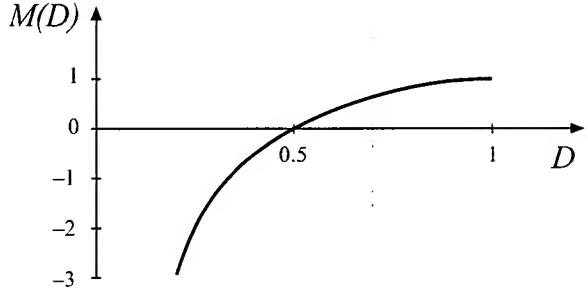
6. *Watkins-Johnson*

$M(D) = \frac{2D-1}{D}$



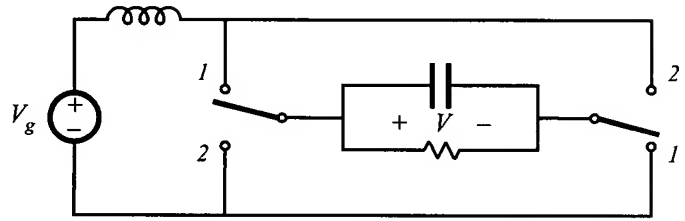
or

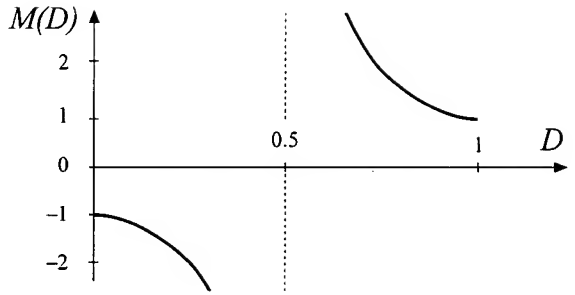




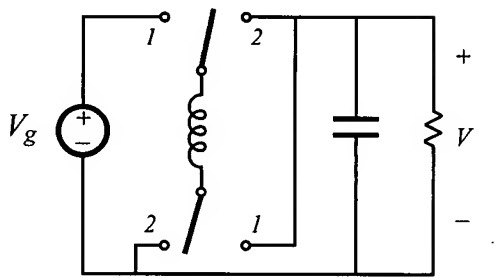
Converters producing a bipolar output voltage suitable as ac-dc rectifiers

7. *Current-fed bridge* $M(D) = \frac{1}{2D-1}$

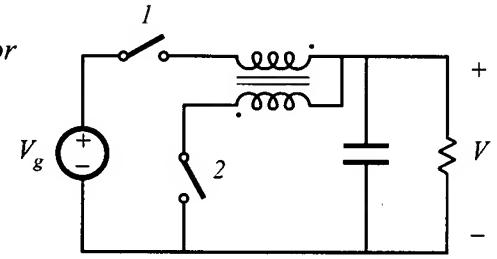


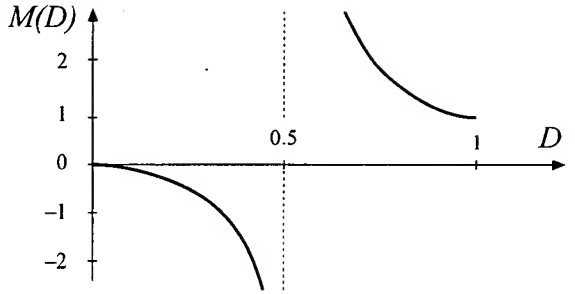


8. *Inverse of Watkins-Johnson* $M(D) = \frac{D}{2D-1}$



or

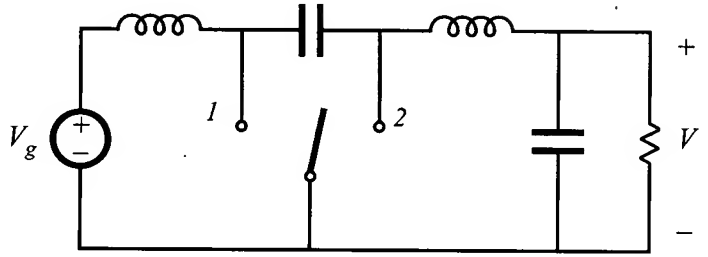


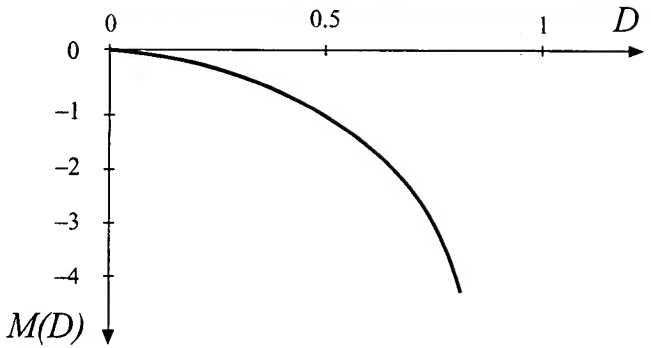


Several members of the class of two-inductor converters

1. *Cuk*

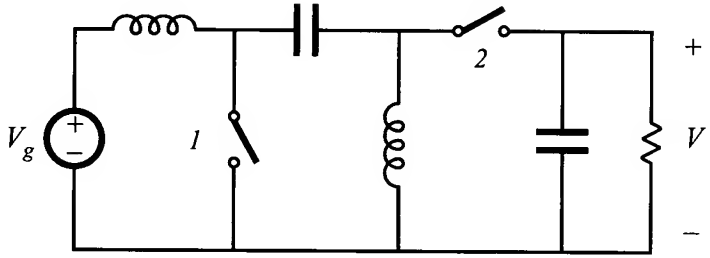
$$M(D) = -\frac{D}{1-D}$$

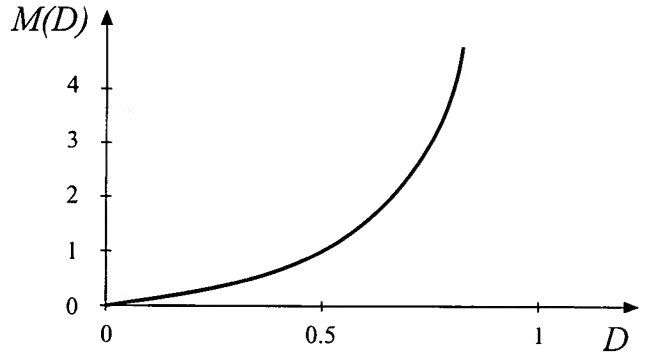




2. *SEPIC*

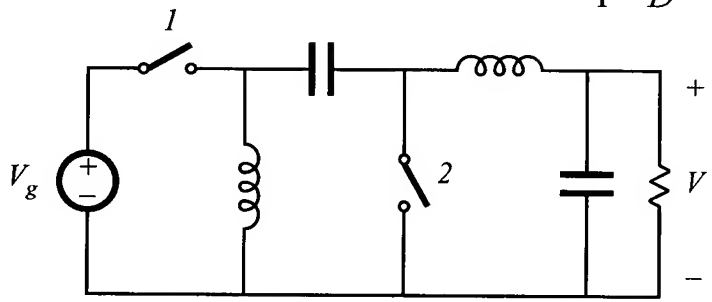
$$M(D) = \frac{D}{1-D}$$

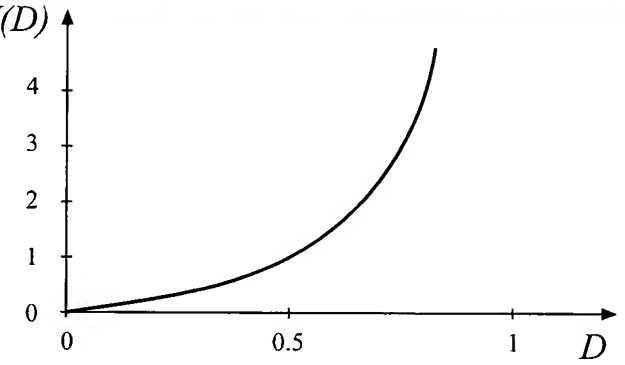




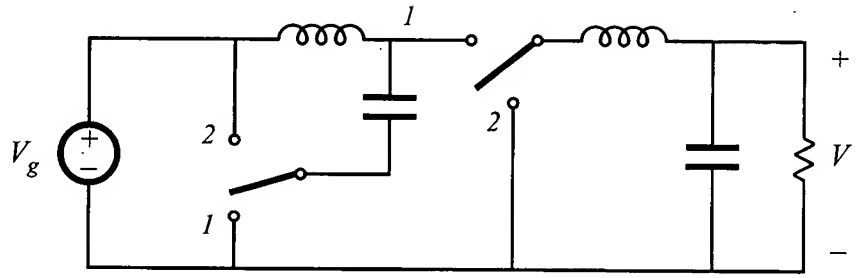
Several members of the class of two-inductor converters

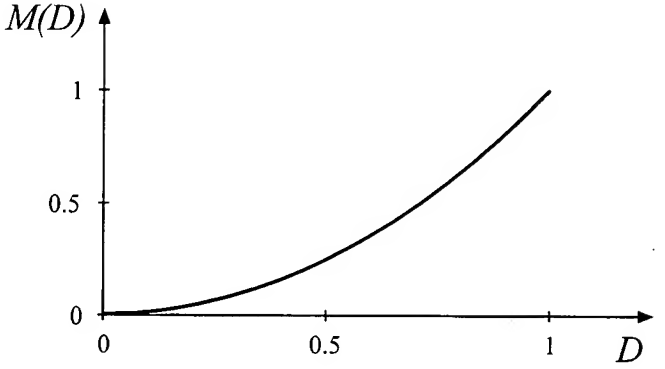
3. *Inverse of SEPIC* $M(D) = \frac{D}{1-D}$





4. *Buck* [2] $M(D) = D^2$





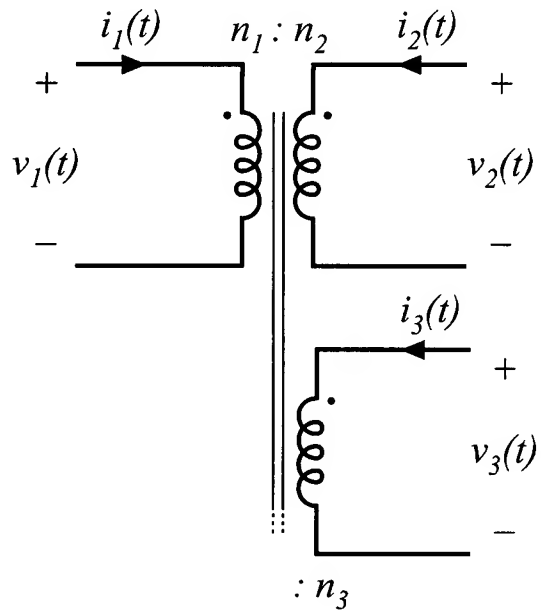
6.3. Transformer isolation

Objectives:

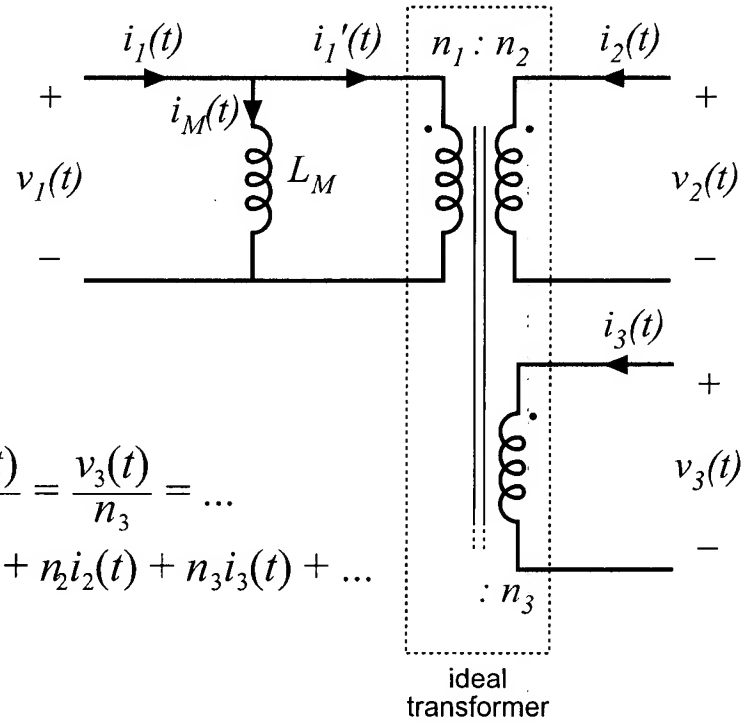
- Isolation of input and output ground connections, to meet safety requirements
- Reduction of transformer size by incorporating high frequency isolation transformer inside converter
- Minimization of current and voltage stresses when a large step-up or step-down conversion ratio is needed — use transformer turns ratio
- Obtain multiple output voltages via multiple transformer secondary windings and multiple converter secondary circuits

A simple transformer model

Multiple winding transformer



Equivalent circuit model

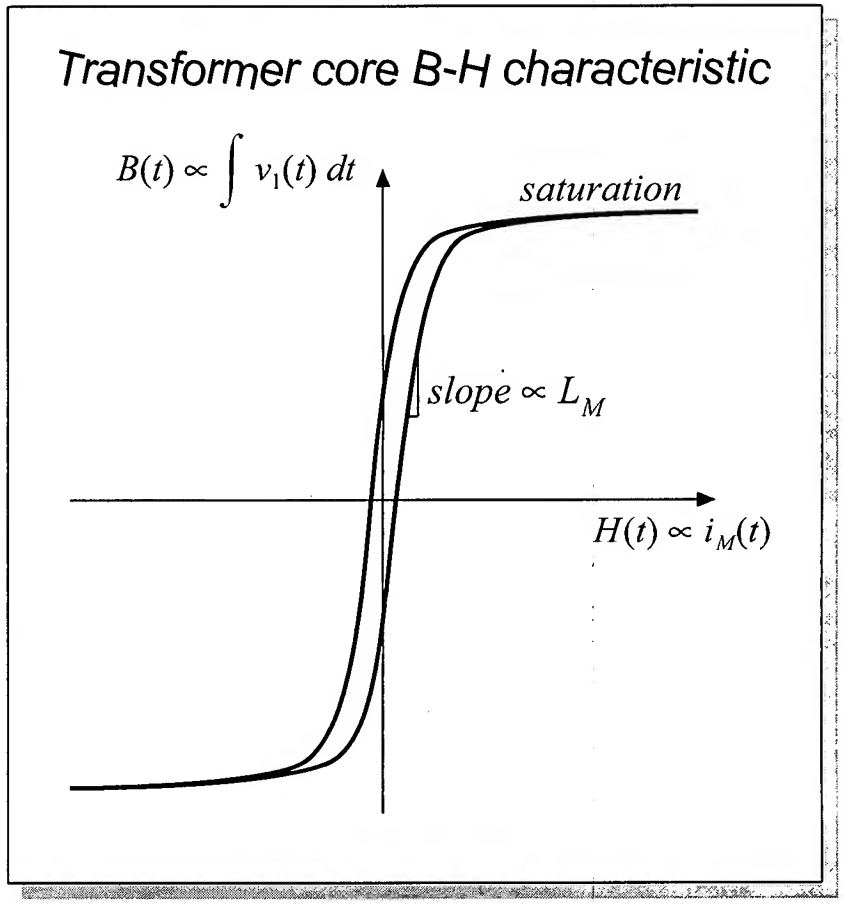


$$\frac{v_1(t)}{n_1} = \frac{v_2(t)}{n_2} = \frac{v_3(t)}{n_3} = \ldots$$

$$0 = n_1 i_1'(t) + n_2 i_2(t) + n_3 i_3(t) + \ldots$$

The magnetizing inductance L_M

- Models magnetization of transformer core material
- Appears effectively in parallel with windings
- If all secondary windings are disconnected, then primary winding behaves as an inductor, equal to the magnetizing inductance
- At dc: magnetizing inductance tends to short-circuit. Transformers cannot pass dc voltages
- Transformer saturates when magnetizing current i_M is too large



Volt-second balance in L_M

The magnetizing inductance is a real inductor, obeying

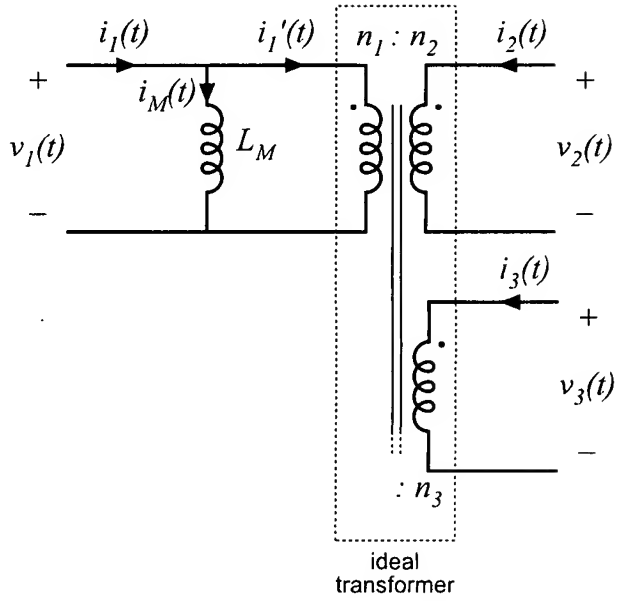
$$v_1(t) = L_M \frac{di_M(t)}{dt}$$

integrate:

$$i_M(t) - i_M(0) = \frac{1}{L_M} \int_0^t v_1(\tau)\, d\tau$$

Magnetizing current is determined by integral of the applied winding voltage. The magnetizing current and the winding currents are independent quantities. Volt-second balance applies: in steady-state, $i_M(T_s) = i_M(0)$, and hence

$$0 = \frac{1}{T_s} \int_0^{T_s} v_1(t)\, dt$$

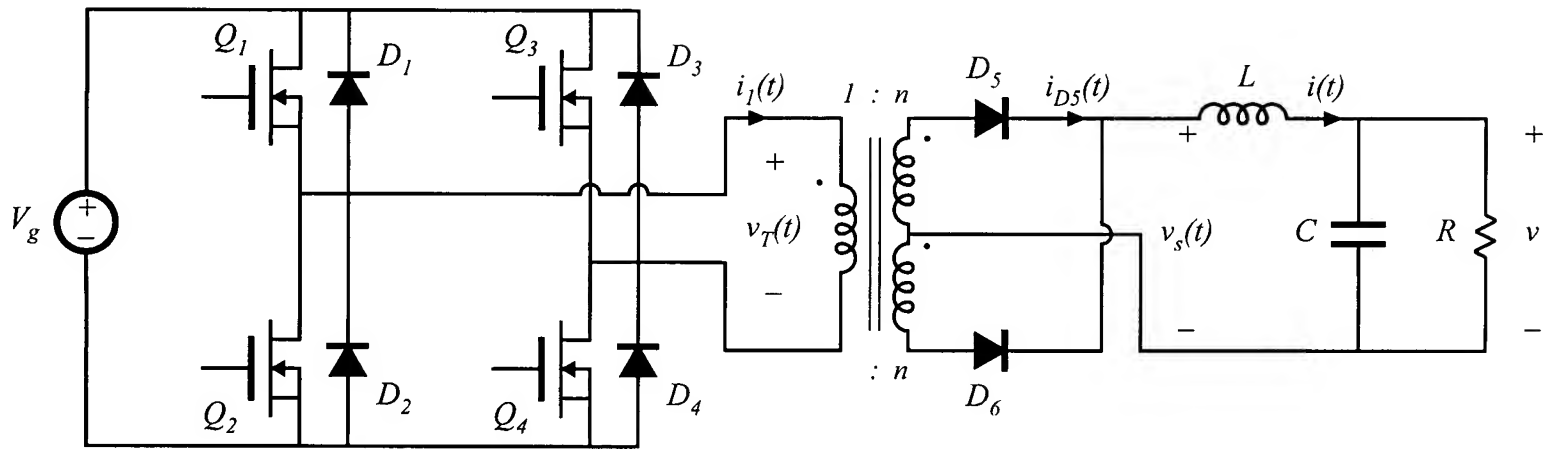


Transformer reset

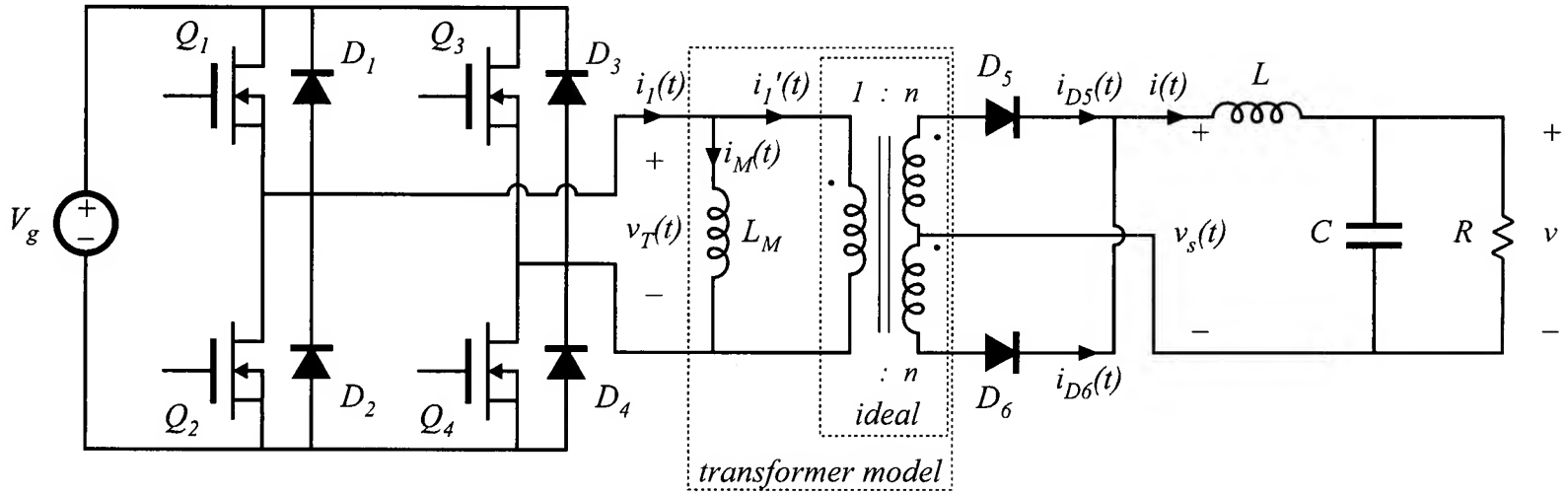
- "Transformer reset" is the mechanism by which magnetizing inductance volt-second balance is obtained
- The need to reset the transformer volt-seconds to zero by the end of each switching period adds considerable complexity to converters
- To understand operation of transformer-isolated converters:
  - replace transformer by equivalent circuit model containing magnetizing inductance
  - analyze converter as usual, treating magnetizing inductance as any other inductor
  - apply volt-second balance to all converter inductors, including magnetizing inductance

6.3.1. Full-bridge and half-bridge isolated buck converters

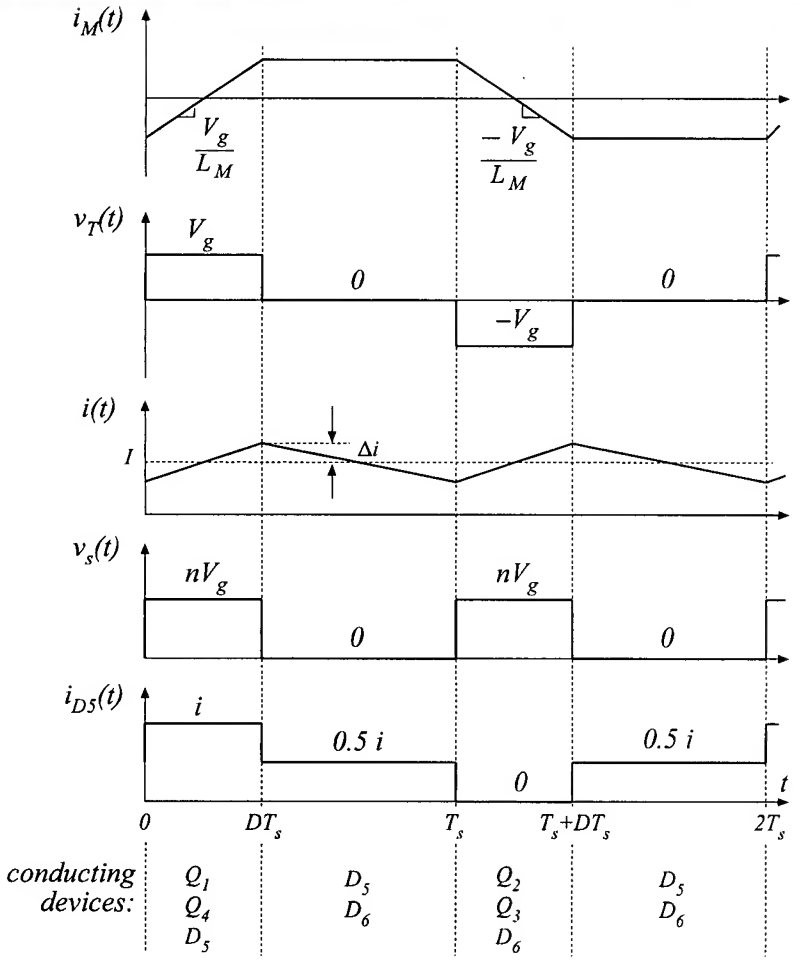
Full-bridge isolated buck converter



Full-bridge, with transformer equivalent circuit



Full-bridge: waveforms



- During first switching period: transistors Q_1 and Q_4 conduct for time DT_s , applying volt-seconds $V_g DT_s$ to primary winding
- During next switching period: transistors Q_2 and Q_3 conduct for time DT_s , applying volt-seconds $-V_g DT_s$ to primary winding
- Transformer volt-second balance is obtained over two switching periods
- Effect of nonidealities?

Effect of nonidealities on transformer volt-second balance

Volt-seconds applied to primary winding during first switching period:

$$(V_g - (Q_1 \text{ and } Q_4 \text{ forward voltage drops}))(Q_1 \text{ and } Q_4 \text{ conduction time})$$

Volt-seconds applied to primary winding during next switching period:

$$-(V_g - (Q_2 \text{ and } Q_3 \text{ forward voltage drops}))(Q_2 \text{ and } Q_3 \text{ conduction time})$$

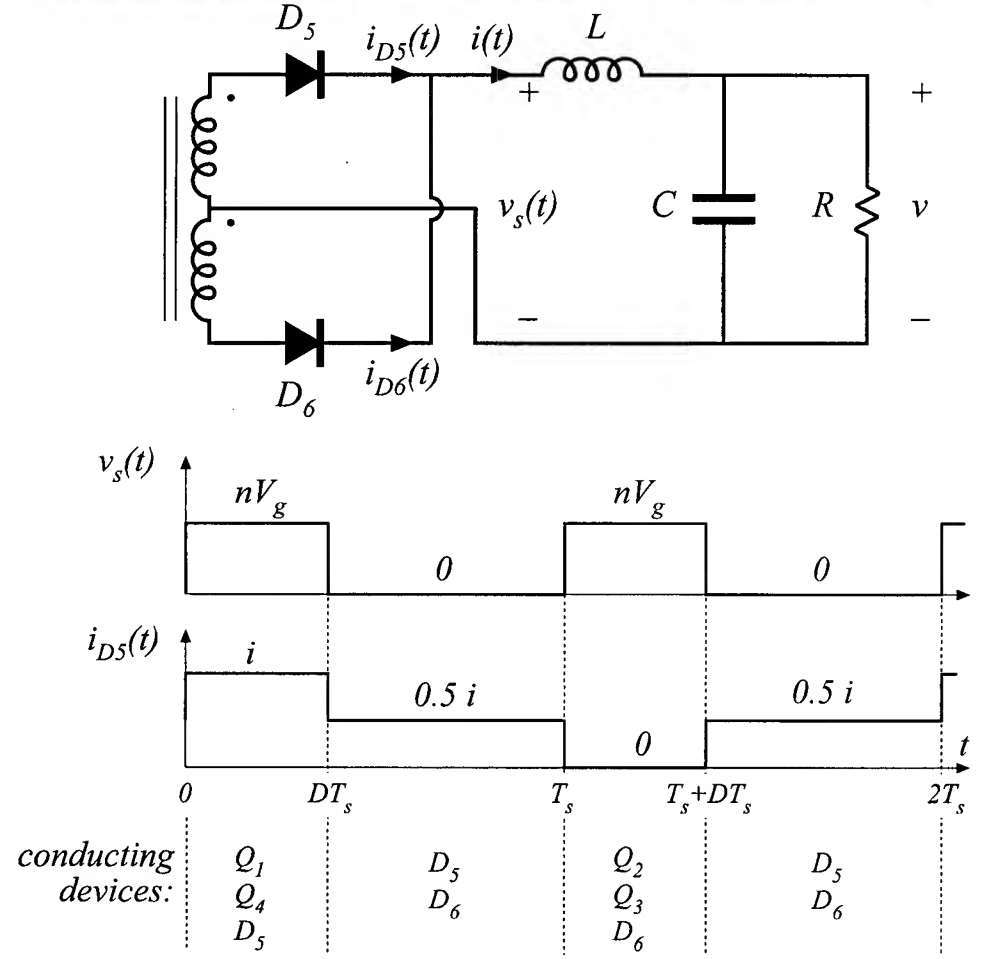
These volt-seconds never add to *exactly* zero.

Net volt-seconds are applied to primary winding

Magnetizing current slowly increases in magnitude

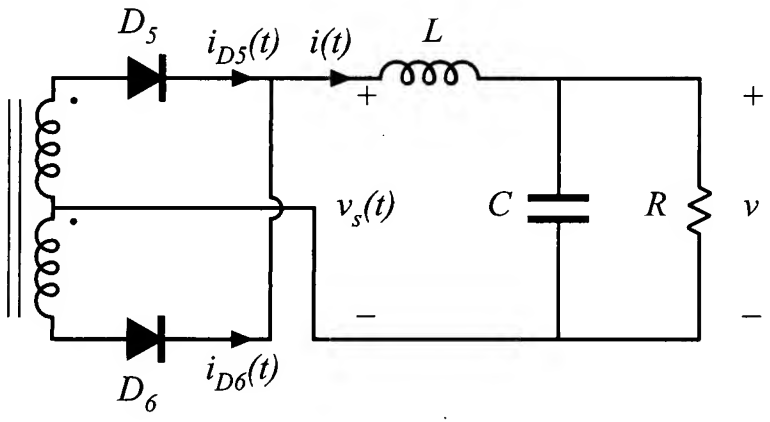
Saturation can be prevented by placing a capacitor in series with primary, or by use of current programmed mode (chapter 11)

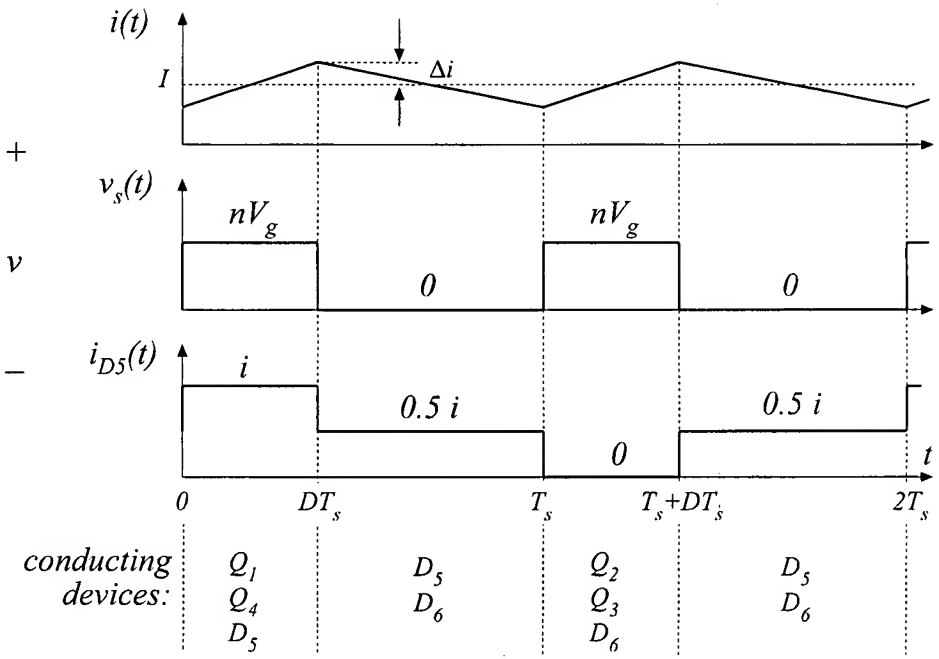
Operation of secondary-side diodes



- During second (D') subinterval, both secondary-side diodes conduct
- Output filter inductor current divides approximately equally between diodes
- Secondary amp-turns add to approximately zero
- Essentially no net magnetization of transformer core by secondary winding currents

Volt-second balance on output filter inductor





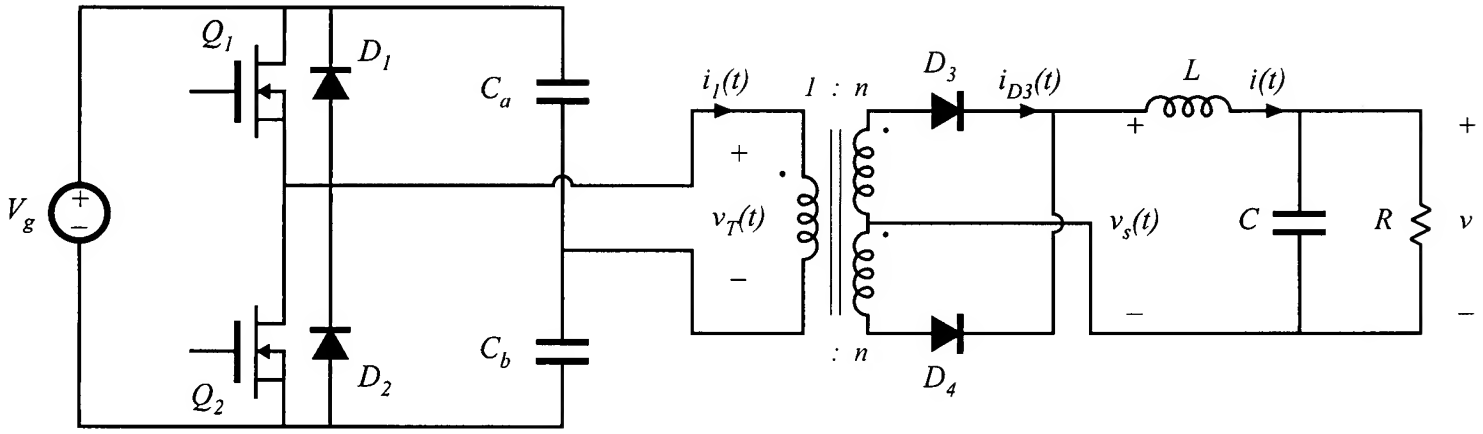
$$V = \langle v_s \rangle$$

$$V = nDV_g$$

$$M(D) = nD$$

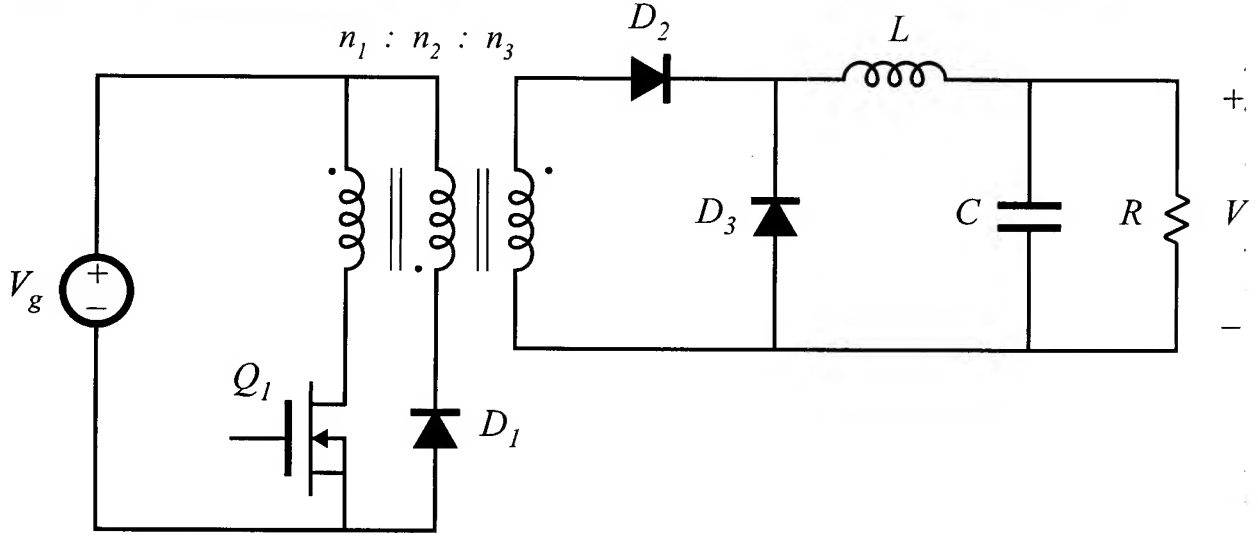
buck converter with turns ratio

Half-bridge isolated buck converter



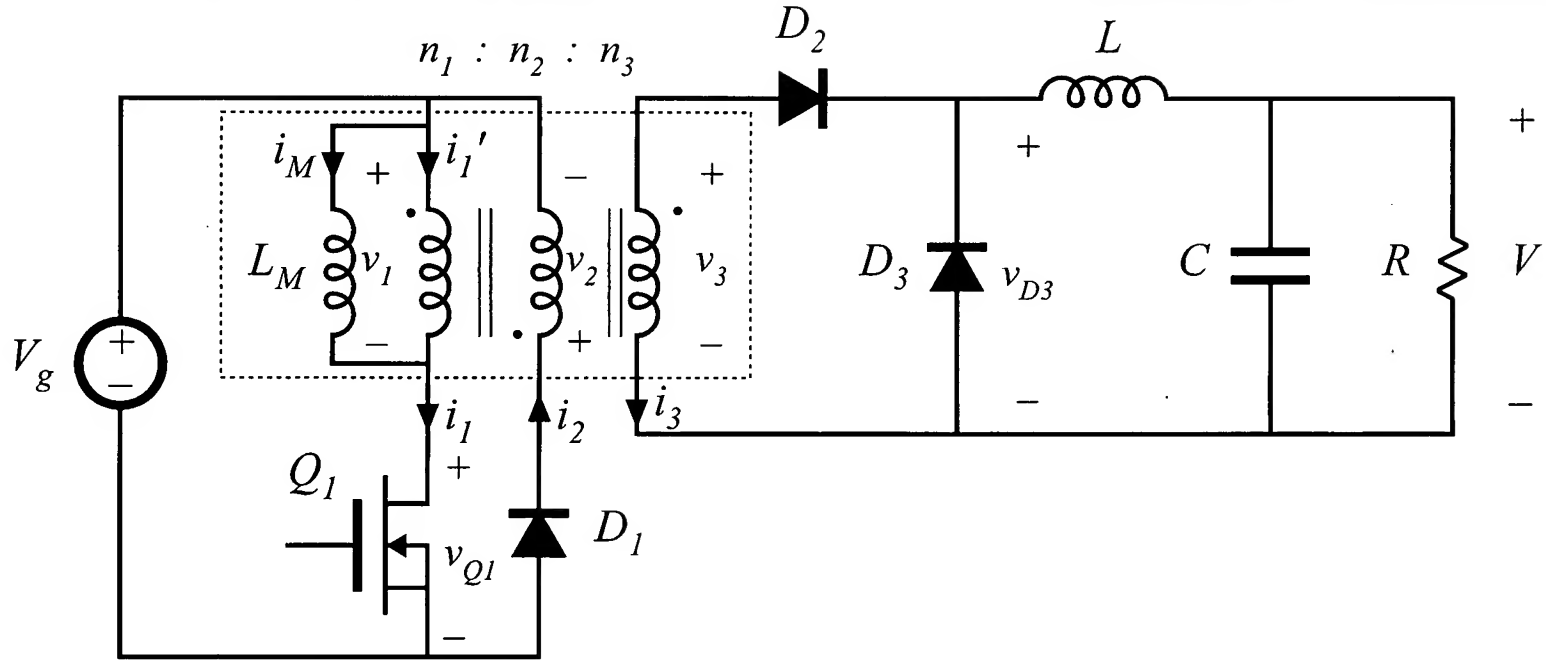
- Replace transistors Q_3 and Q_4 with large capacitors
- Voltage at capacitor centerpoint is $0.5V_g$
- $v_s(t)$ is reduced by a factor of two
- $M = 0.5\,nD$

6.3.2. Forward converter

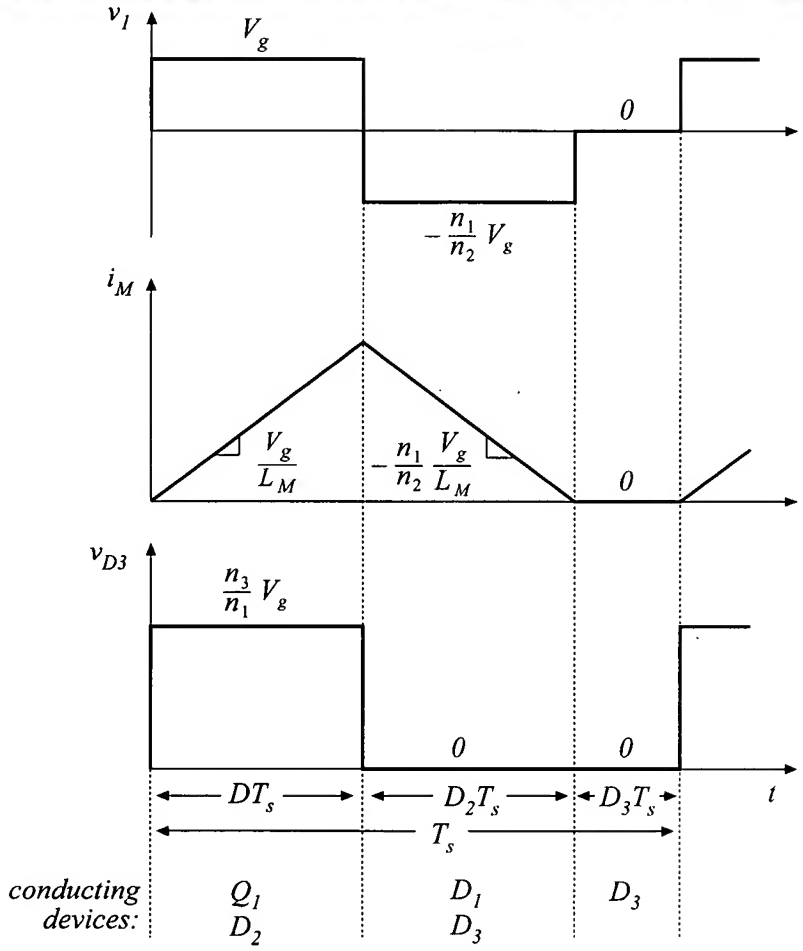


- Buck-derived transformer-isolated converter
- Single-transistor and two-transistor versions
- Maximum duty cycle is limited
- Transformer is reset while transistor is off

Forward converter with transformer equivalent circuit

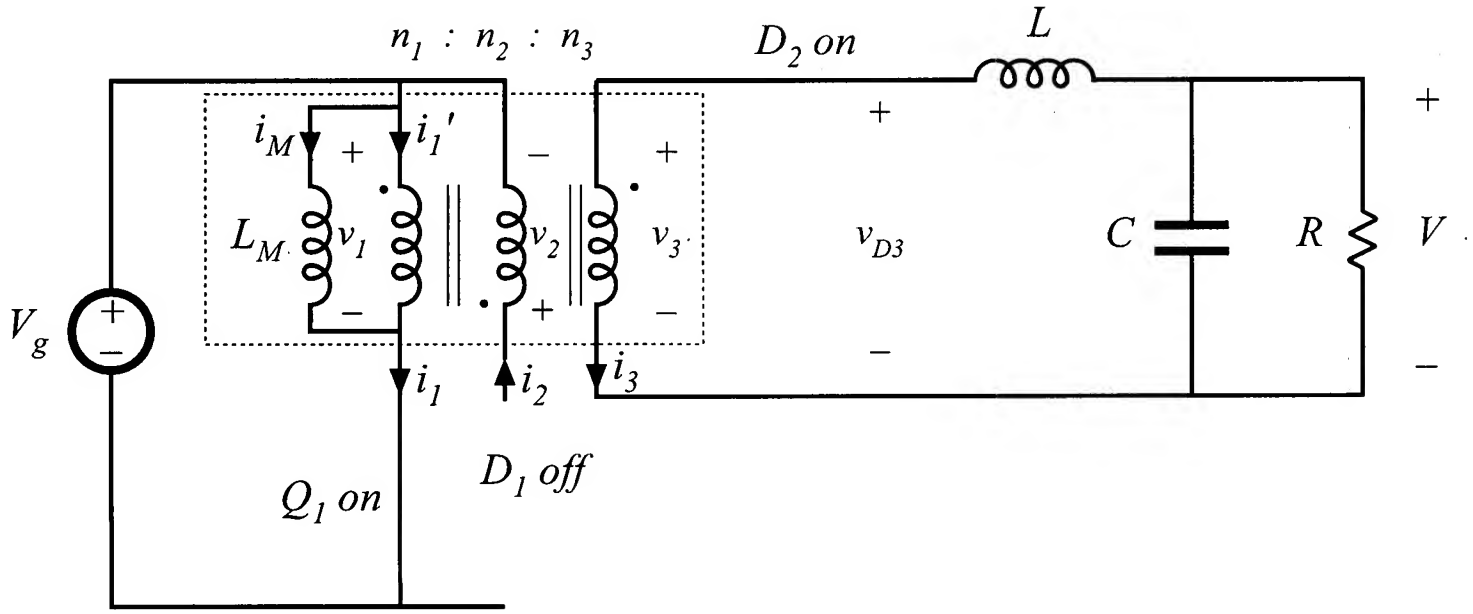


Forward converter: waveforms

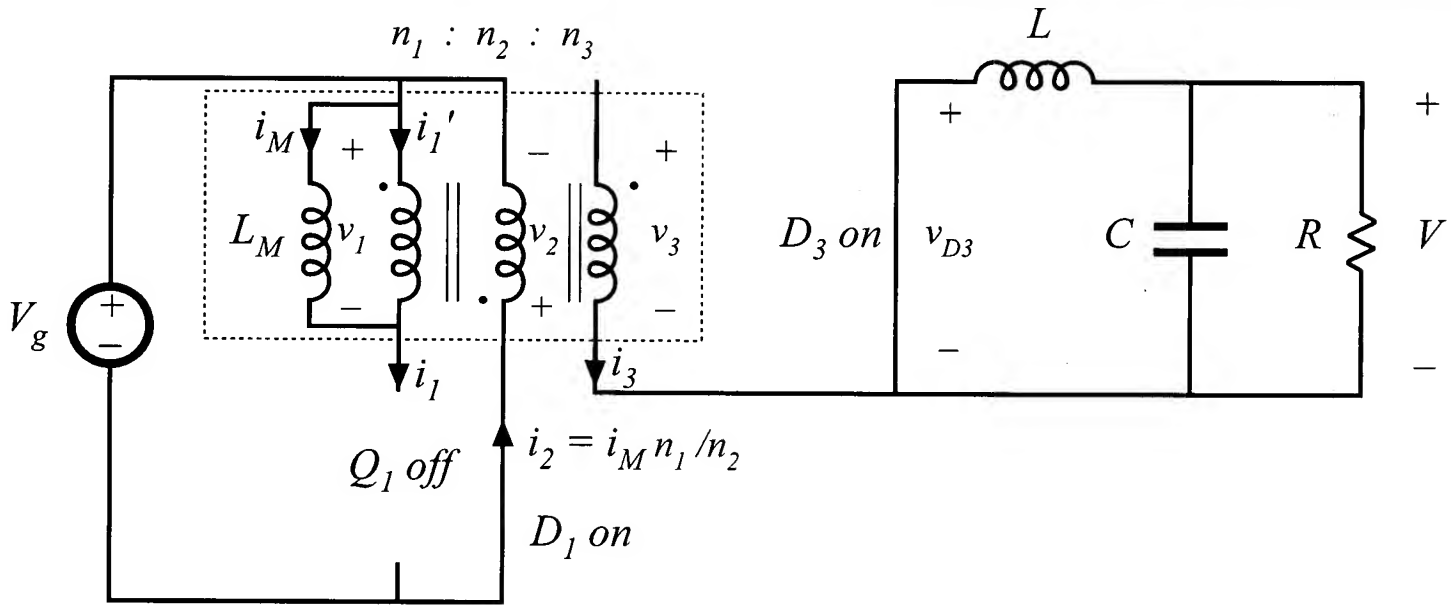


- Magnetizing current, in conjunction with diode D_1, operates in discontinuous conduction mode
- Output filter inductor, in conjunction with diode D_3, may operate in either CCM or DCM

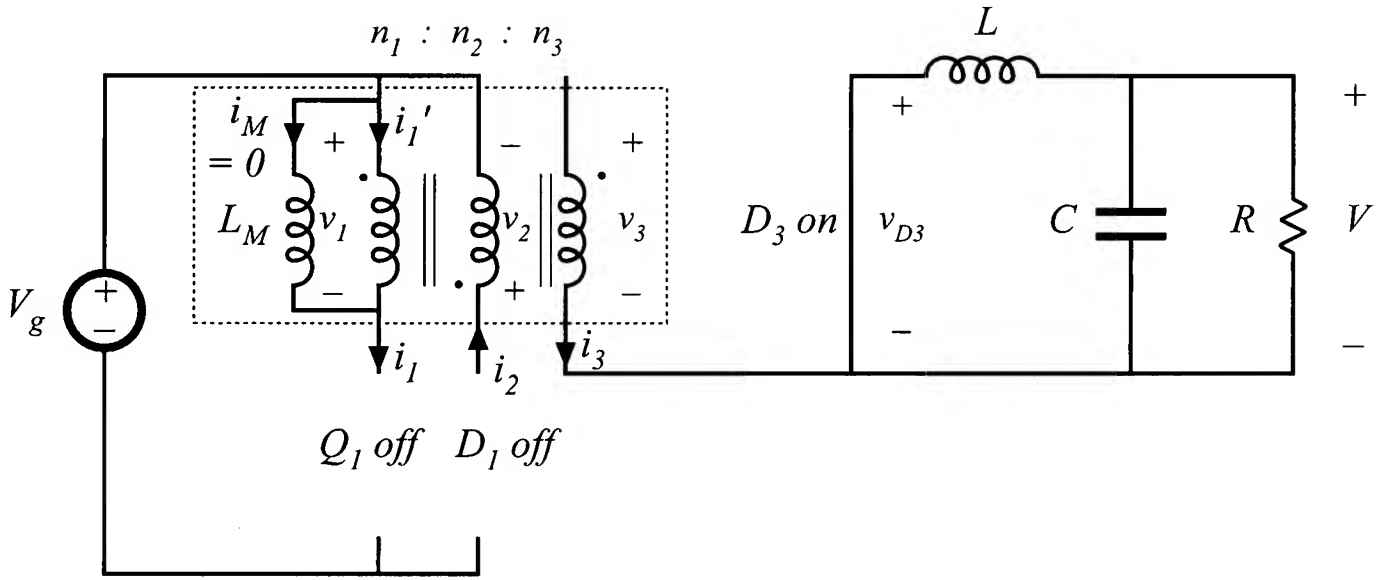
Subinterval 1: transistor conducts



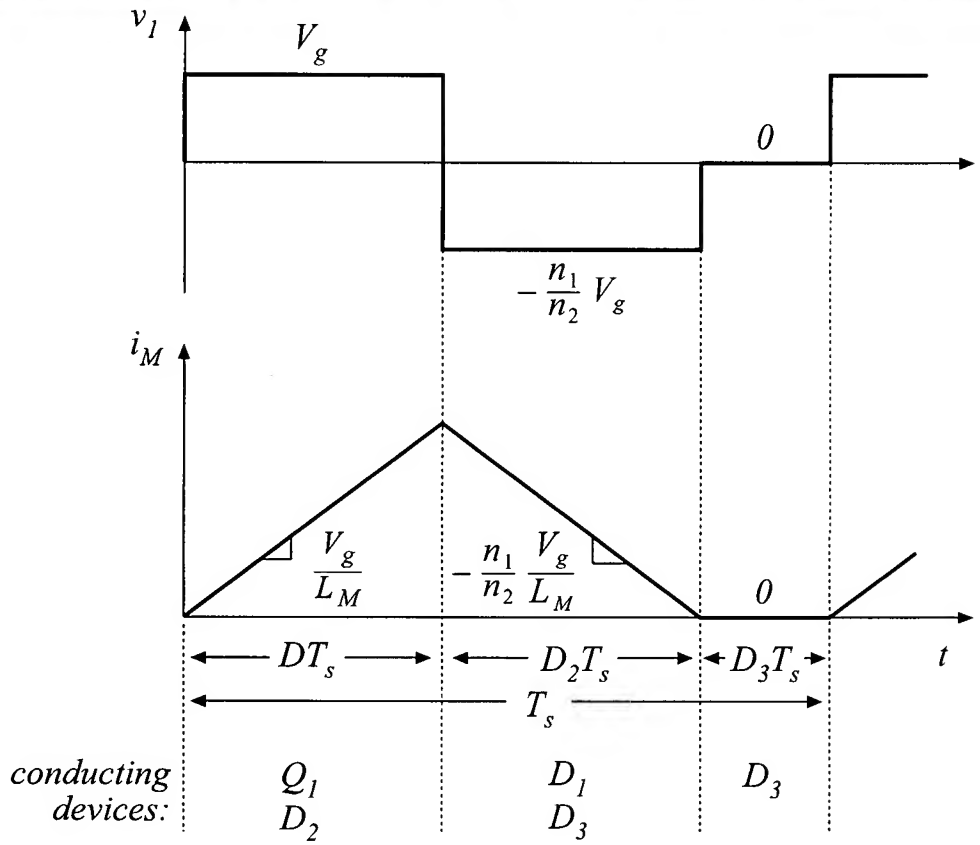
Subinterval 2: transformer reset



Subinterval 3



Magnetizing inductance volt-second balance



$$\langle v_1 \rangle = D\,(\,V_g\,) + D_2\,(\,-V_g\,n_1 / n_2\,) + D_3\,(\,0\,) = 0$$

Transformer reset

From magnetizing current volt-second balance:

$$\langle v_1 \rangle = D\,(\,V_g\,) + D_2\,(\,-V_g\,n_1 / n_2\,) + D_3\,(\,0\,) = 0$$

Solve for D_2:

$$D_2 = \frac{n_2}{n_1} D$$

D_3 cannot be negative. But $D_3 = 1 - D - D_2$. Hence

$$D_3 = 1 - D - D_2 \geq 0$$

$$D_3 = 1 - D\left(1 + \frac{n_2}{n_1}\right) \geq 0$$

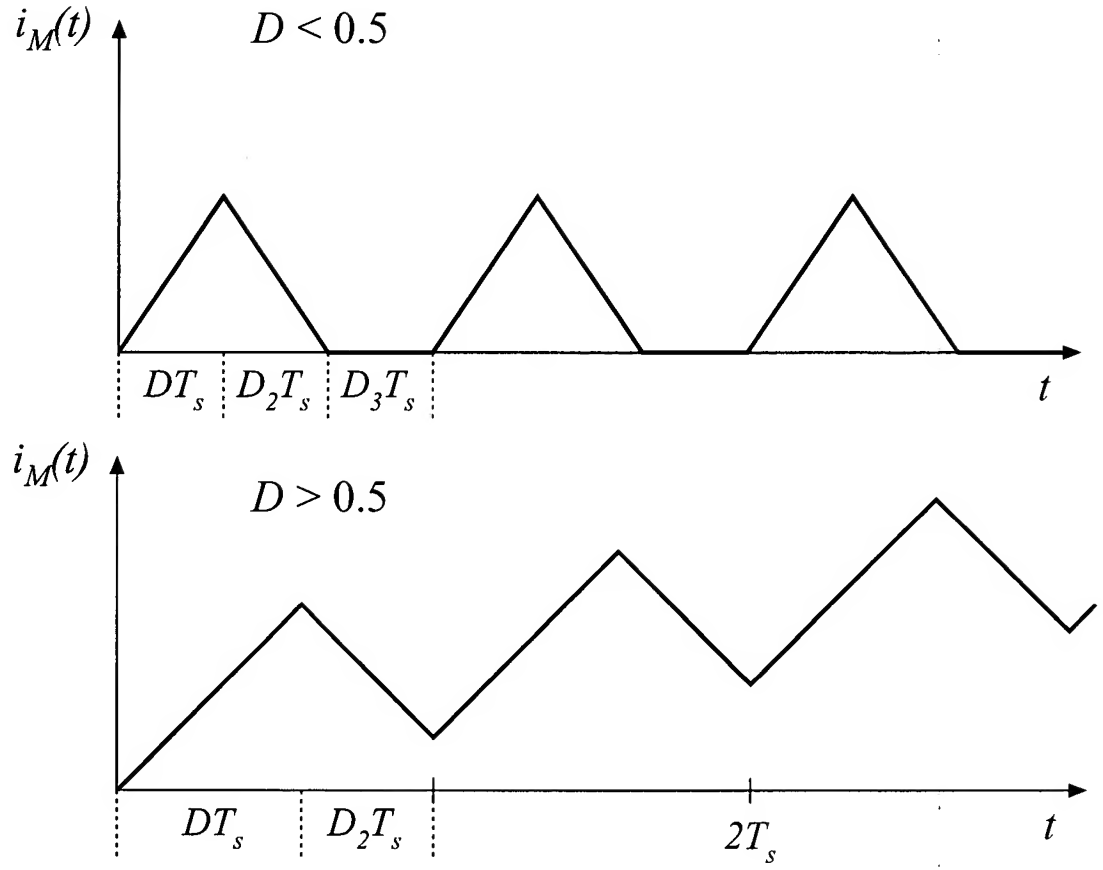
Solve for D

$$D \leq \frac{1}{1 + \frac{n_2}{n_1}}$$

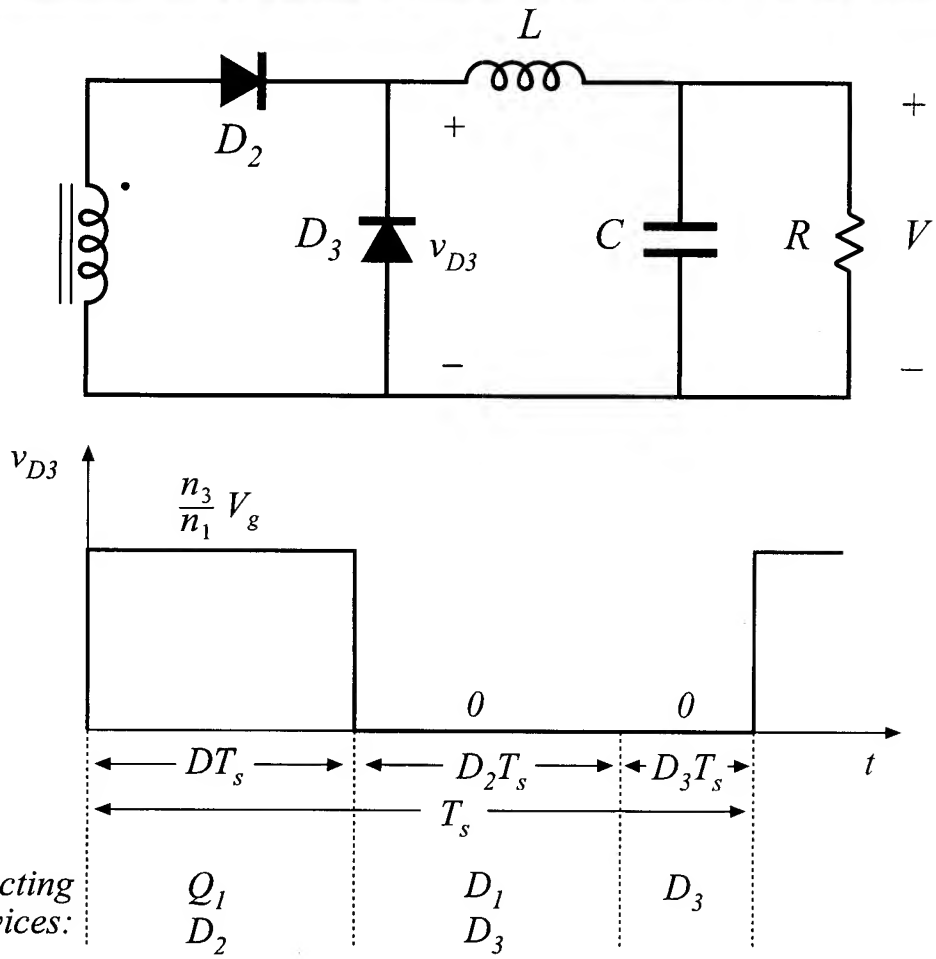
for $n_1 = n_2$: $D \leq \frac{1}{2}$

What happens when $D > 0.5$

magnetizing current waveforms, for $n_1 = n_2$



Conversion ratio *M(D)*



$$\langle v_{D3} \rangle = V = \frac{n_3}{n_1} D V_g$$

Maximum duty cycle vs. transistor voltage stress

Maximum duty cycle limited to

$$D \leq \frac{1}{1 + \frac{n_2}{n_1}}$$

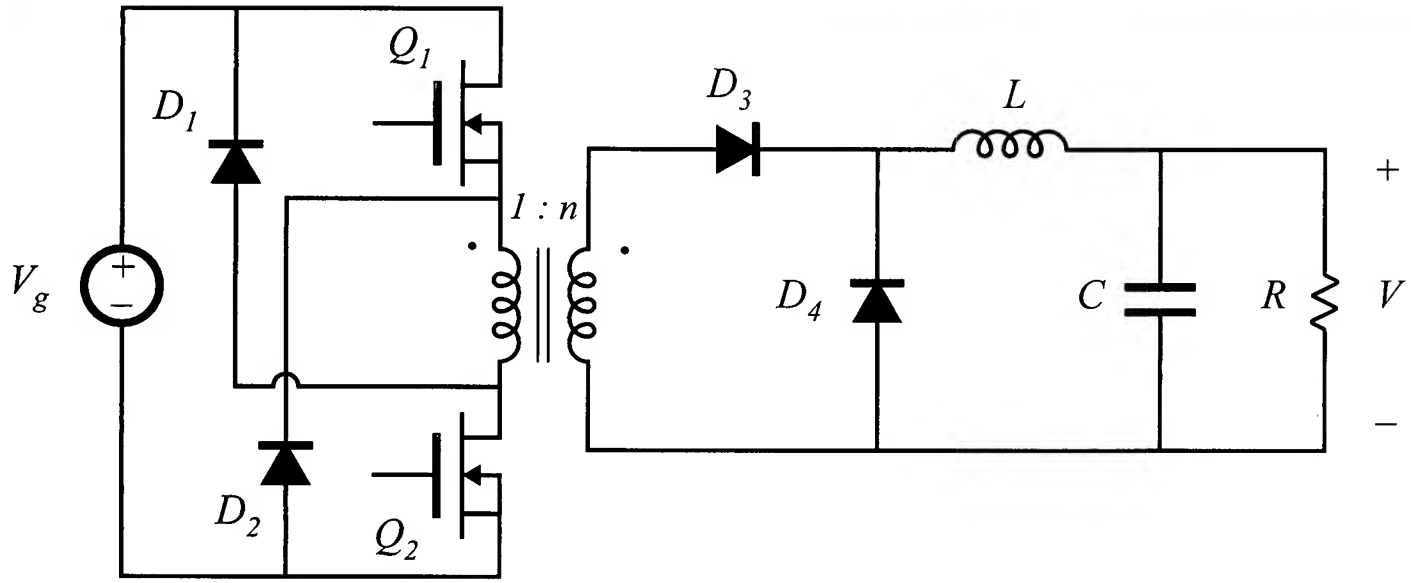
which can be increased by increasing the turns ratio n_2 / n_1. But this increases the peak transistor voltage:

$$\max v_{Q1} = V_g \left(1 + \frac{n_1}{n_2} \right)$$

For $n_1 = n_2$

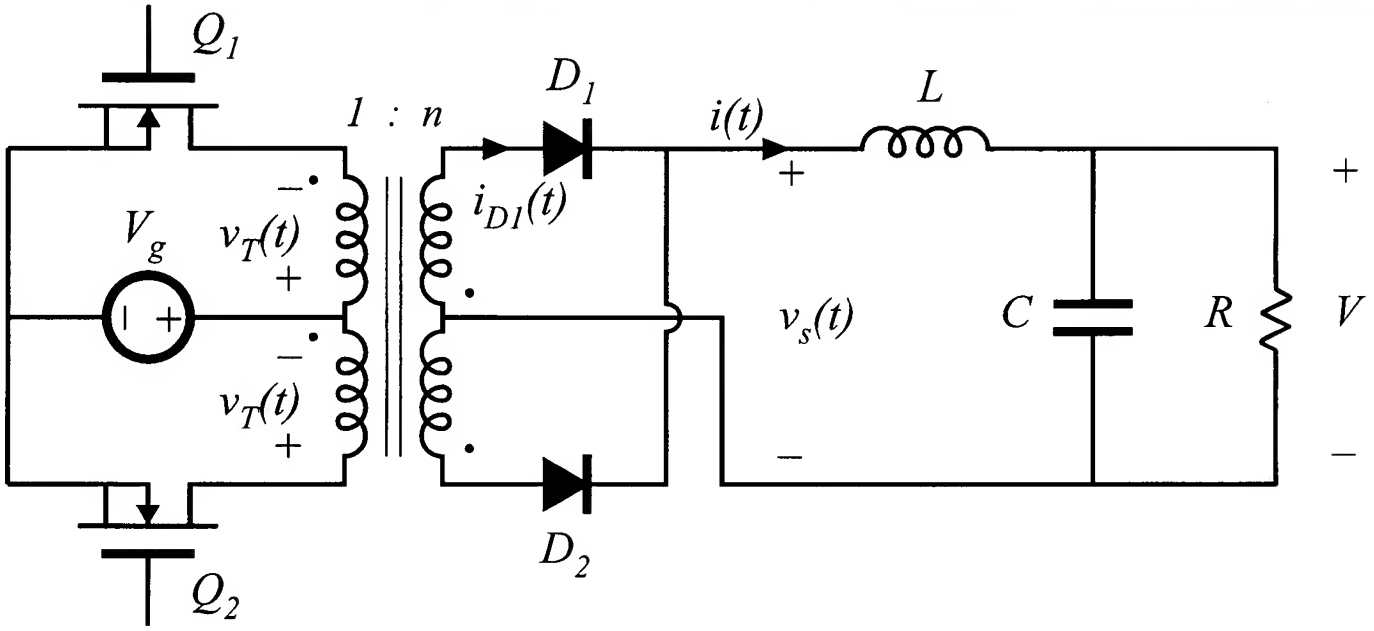
$$D \leq \frac{1}{2} \qquad \text{and} \qquad \max v_{Q1} = 2V_g$$

The two-transistor forward converter



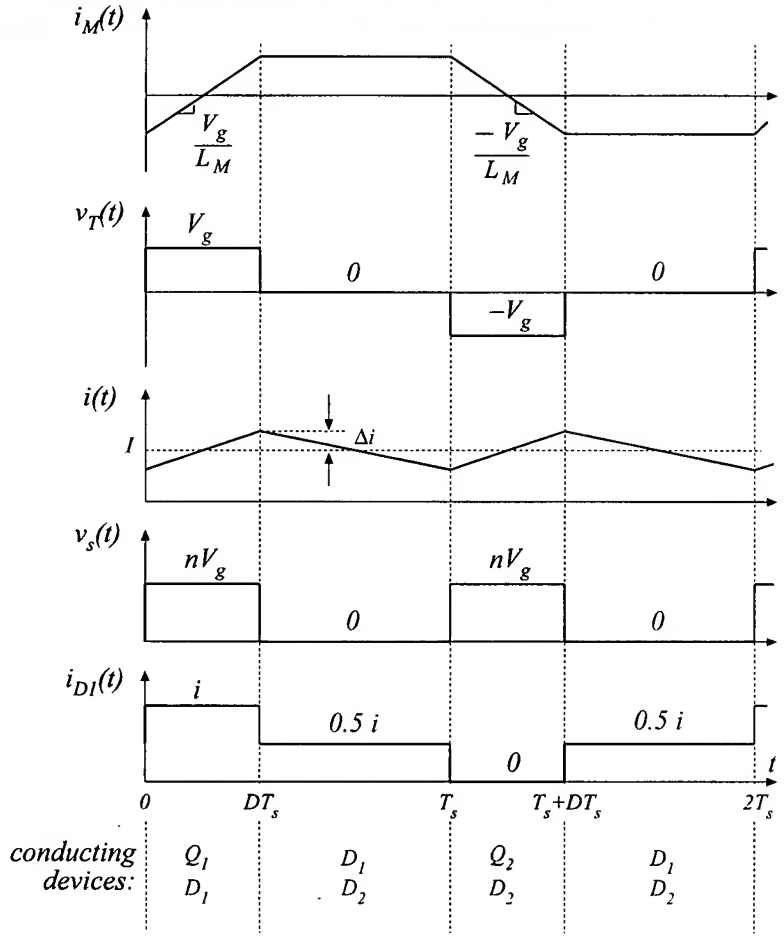
$$V = nDV_g \qquad D \le \frac{1}{2} \qquad \max v_{Q1} = \max v_{Q2} = V_g$$

6.3.3. Push-pull isolated buck converter



$$V = nDV_g \qquad 0 \le D \le 1$$

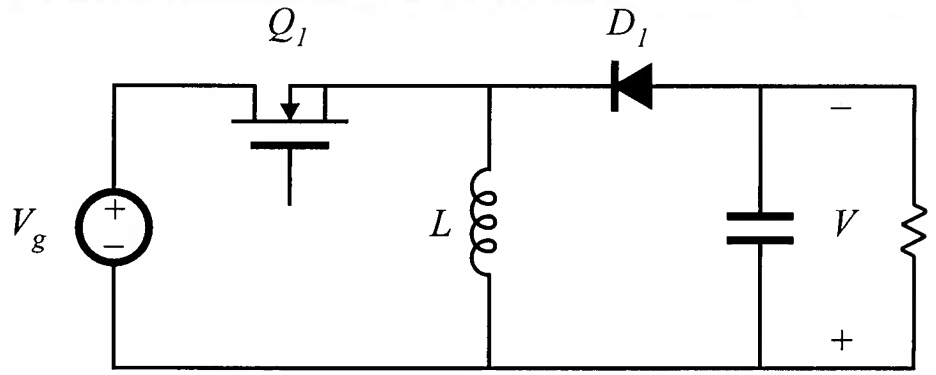
Waveforms: push-pull



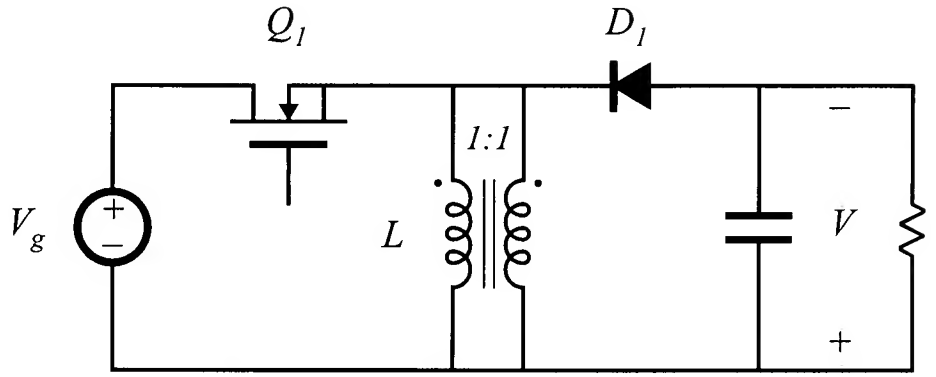
- Used with low-voltage inputs
- Secondary-side circuit identical to full bridge
- As in full bridge, transformer volt-second balance is obtained over two switching periods
- Effect of nonidealities on transformer volt-second balance?
- Current programmed control can be used to mitigate transformer saturation problems. Duty cycle control not recommended.

6.3.4. Flyback converter

buck-boost converter:

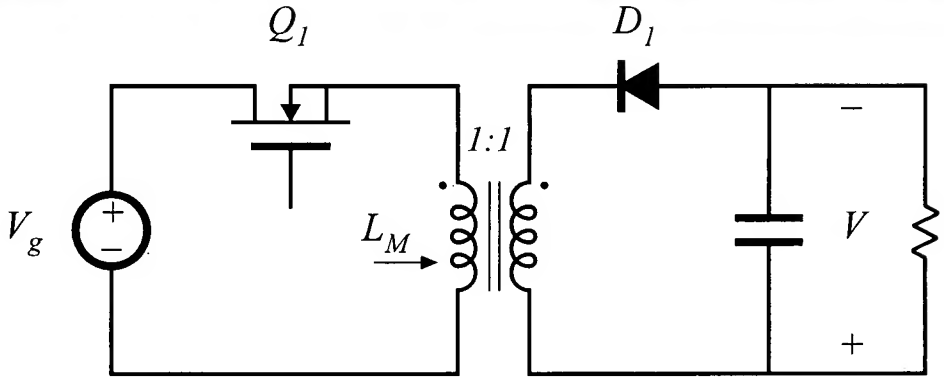


construct inductor winding using two parallel wires:

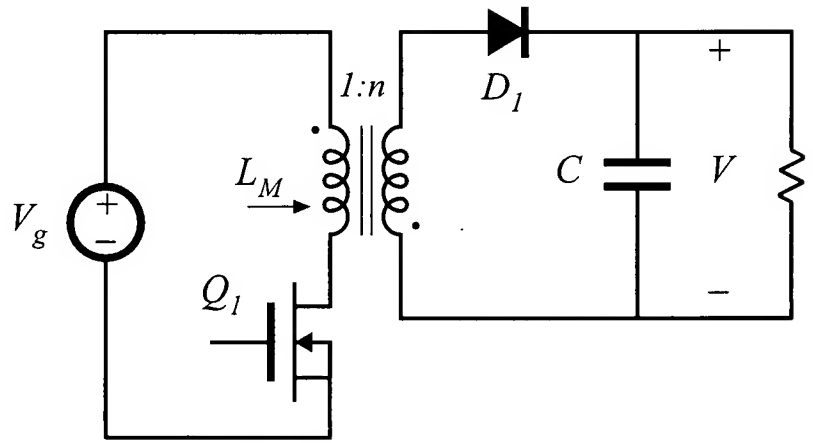


Derivation of flyback converter, cont.

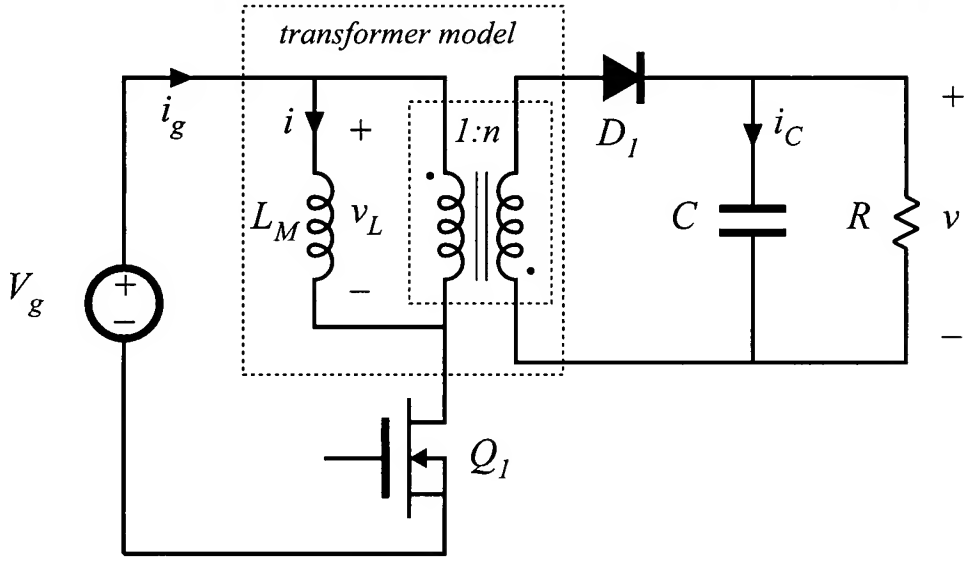
Isolate inductor windings: the flyback converter



Flyback converter having a 1:n turns ratio and positive output:



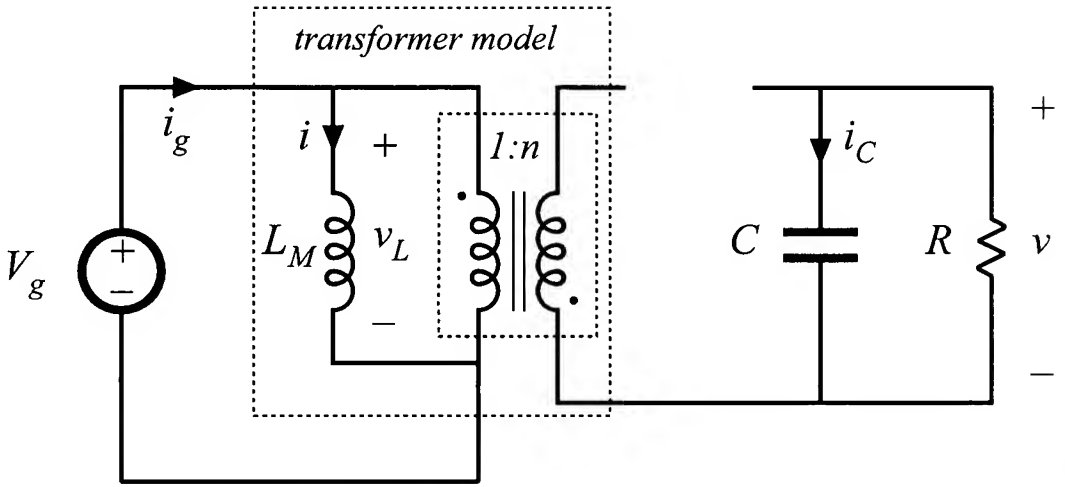
The "flyback transformer"



- A two-winding inductor
- Symbol is same as transformer, but function differs significantly from ideal transformer
- Energy is stored in magnetizing inductance
- Magnetizing inductance is relatively small

- Current does not simultaneously flow in primary and secondary windings
- Instantaneous winding voltages follow turns ratio
- Instantaneous (and rms) winding currents do not follow turns ratio
- Model as (small) magnetizing inductance in parallel with ideal transformer

Subinterval 1

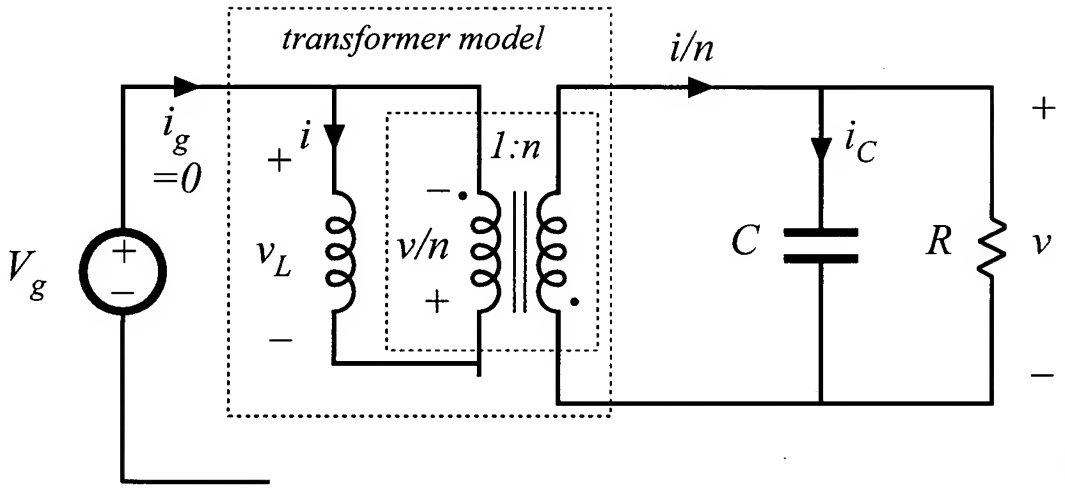


$$v_L = V_g$$
$$i_C = -\frac{v}{R}$$
$$i_g = i$$

CCM: small ripple approximation leads to

$$v_L = V_g$$
$$i_C = -\frac{V}{R}$$
$$i_g = I$$

Subinterval 2



$$v_L = -\frac{v}{n}$$

$$i_C = \frac{i}{n} - \frac{v}{R}$$

$$i_g = 0$$

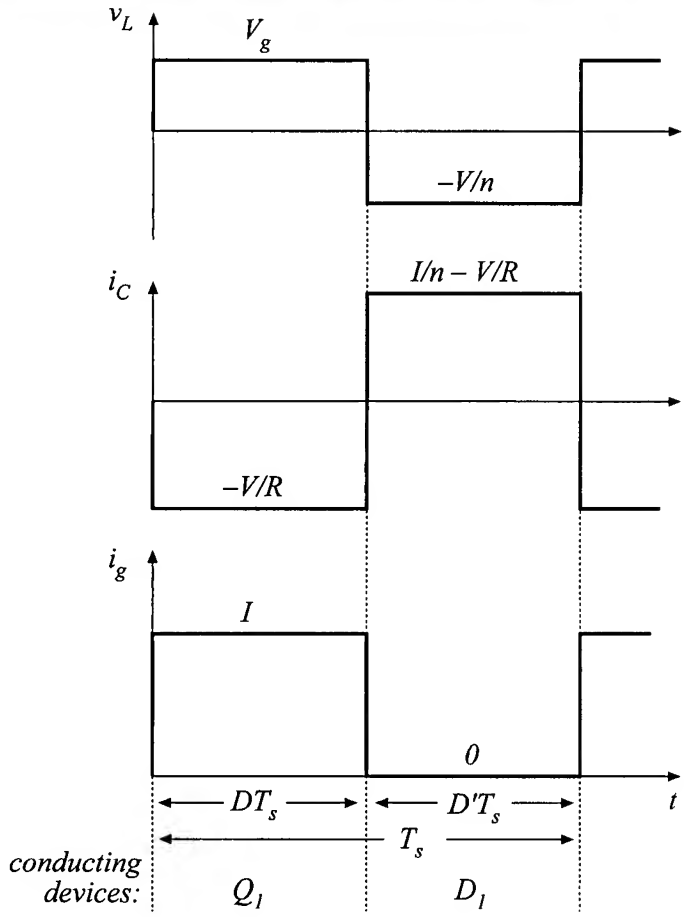
CCM: small ripple approximation leads to

$$v_L = -\frac{V}{n}$$

$$i_C = \frac{I}{n} - \frac{V}{R}$$

$$i_g = 0$$

CCM Flyback waveforms and solution



Volt-second balance:

$$\langle v_L \rangle = D\,(V_g) + D'\,(-\frac{V}{n}) = 0$$

Conversion ratio is

$$M(D) = \frac{V}{V_g} = n\,\frac{D}{D'}$$

Charge balance:

$$\langle i_C \rangle = D\,(-\frac{V}{R}) + D'\,(\frac{I}{n} - \frac{V}{R}) = 0$$

Dc component of magnetizing current is

$$I = \frac{nV}{D'R}$$

Dc component of source current is

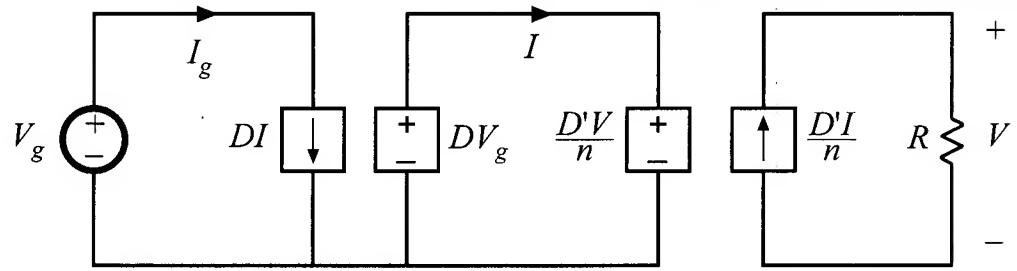
$$I_g = \langle i_g \rangle = D\,(I) + D'\,(0)$$

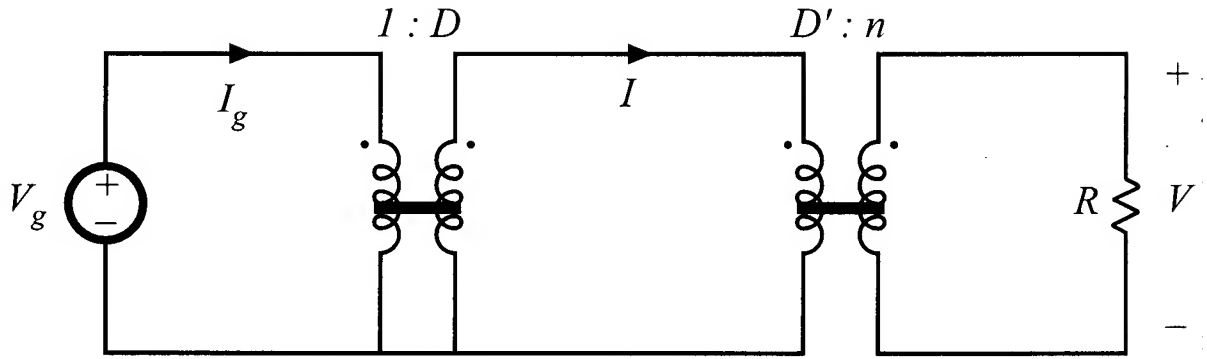
Equivalent circuit model: CCM Flyback

$$\langle v_L \rangle = D\,(V_g) + D'\,(-\frac{V}{n}) = 0$$

$$\langle i_C \rangle = D\,(-\frac{V}{R}) + D'\,(\frac{I}{n} - \frac{V}{R}) = 0$$

$$I_g = \langle i_g \rangle = D\,(I) + D'\,(0)$$





Discussion: Flyback converter

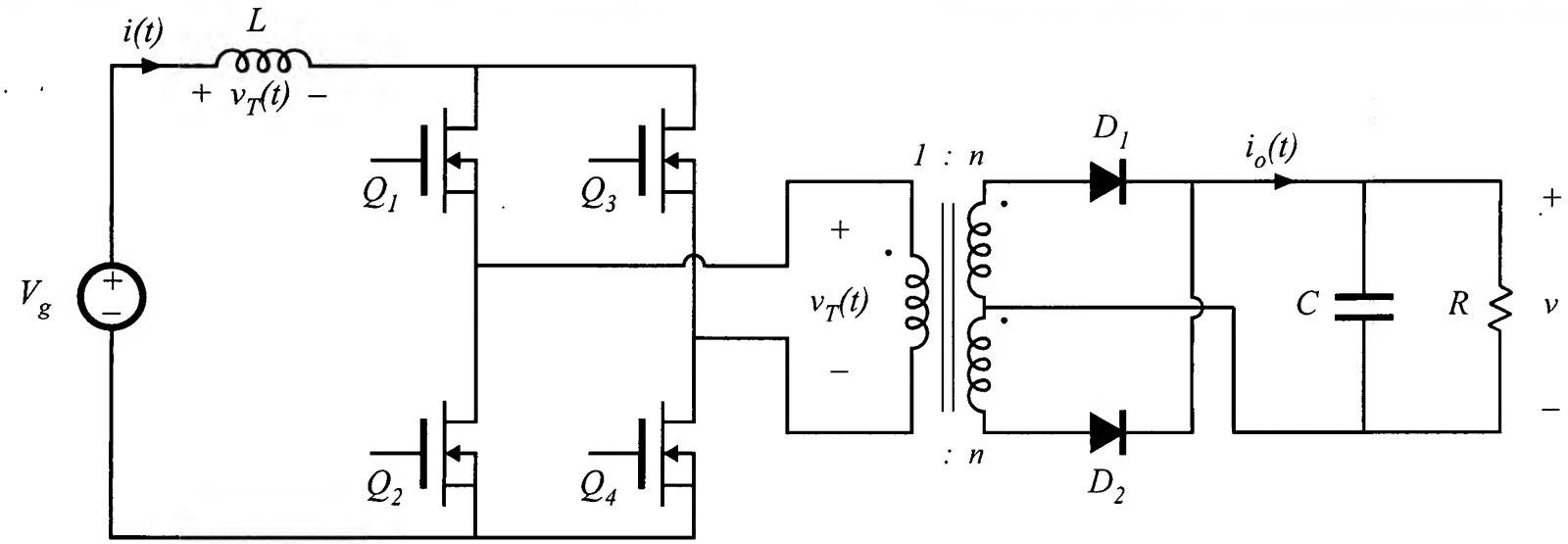
- Widely used in low power and/or high voltage applications
- Low parts count
- Multiple outputs are easily obtained, with minimum additional parts
- Cross regulation is inferior to buck-derived isolated converters
- Often operated in discontinuous conduction mode
- DCM analysis: DCM buck-boost with turns ratio

6.3.5. Boost-derived isolated converters

- A wide variety of boost-derived isolated dc-dc converters can be derived, by inversion of source and load of buck-derived isolated converters:
  - full-bridge and half-bridge isolated boost converters
  - inverse of forward converter: the "reverse" converter
  - push-pull boost-derived converter

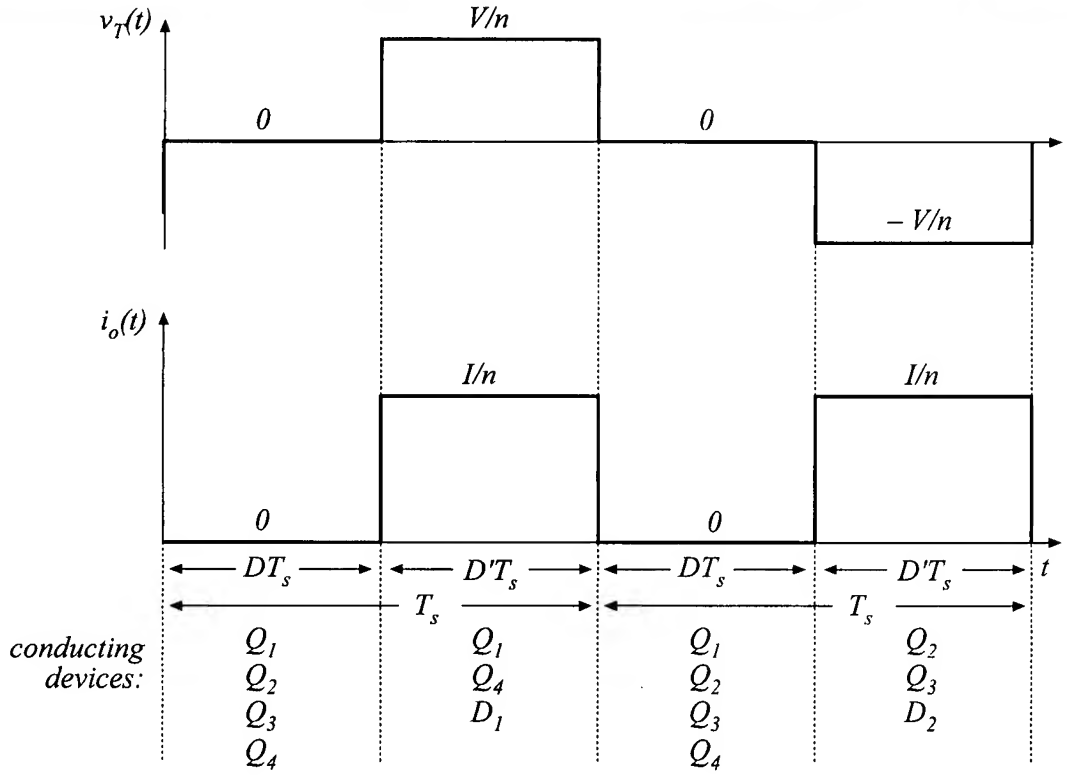
Of these, the full-bridge and push-pull boost-derived isolated converters are the most popular, and are briefly discussed here.

Full-bridge transformer-isolated boost-derived converter



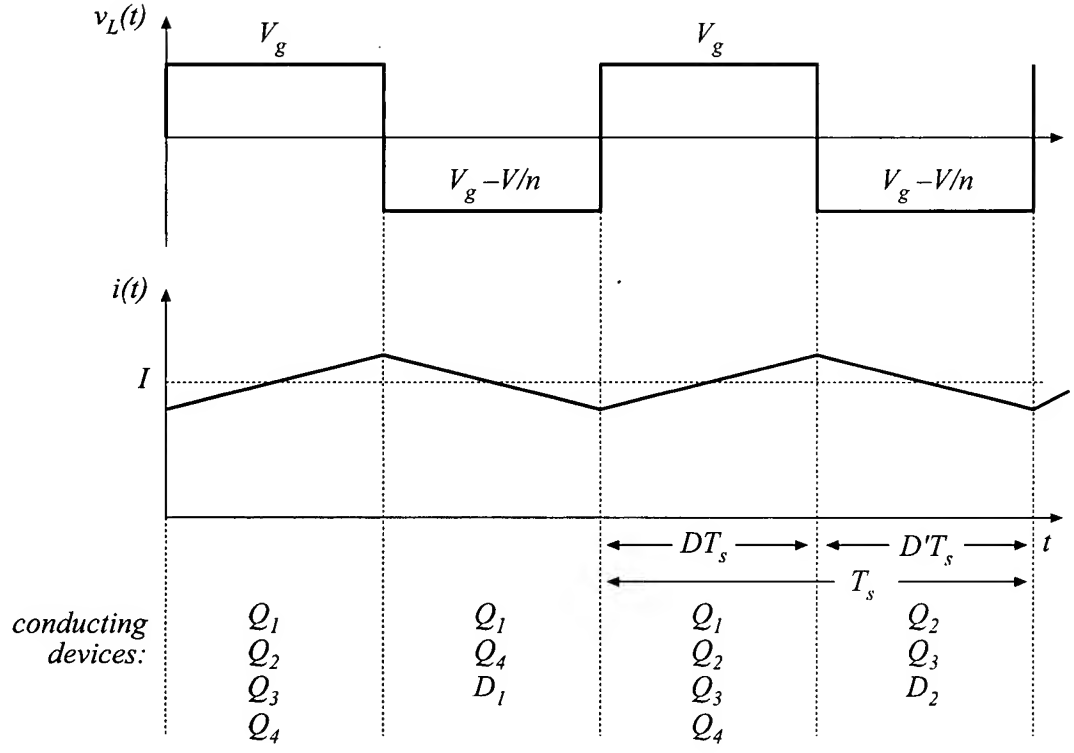
- Circuit topologies are equivalent to those of nonisolated boost converter
- With 1:1 turns ratio, inductor current $i(t)$ and output current $i_o(t)$ waveforms are identical to nonisolated boost converter

Transformer reset mechanism



- As in full-bridge buck topology, transformer volt-second balance is obtained over two switching periods.
- During first switching period: transistors Q_1 and Q_4 conduct for time DT_s, applying volt-seconds VDT_s to secondary winding.
- During next switching period: transistors Q_2 and Q_3 conduct for time DT_s, applying volt-seconds $-VDT_s$ to secondary winding.

Conversion ratio *M(D)*



Application of volt-second balance to inductor voltage waveform:

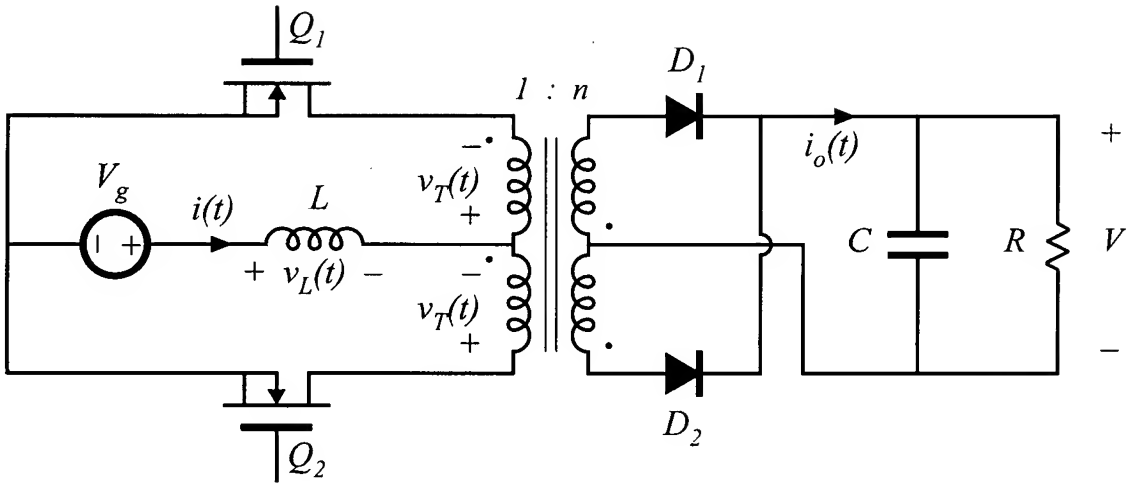
$$\langle v_L \rangle = D\,(V_g) + D'\,(V_g - V/n) = 0$$

Solve for *M(D)*:

$$M(D) = \frac{V}{V_g} = \frac{n}{D'}$$

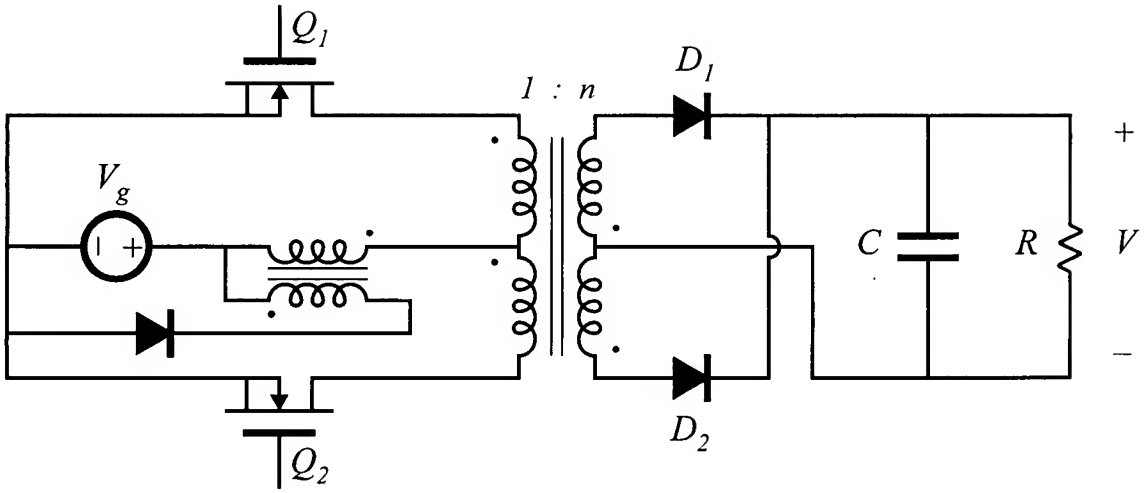
—boost with turns ratio n

Push-pull boost-derived converter



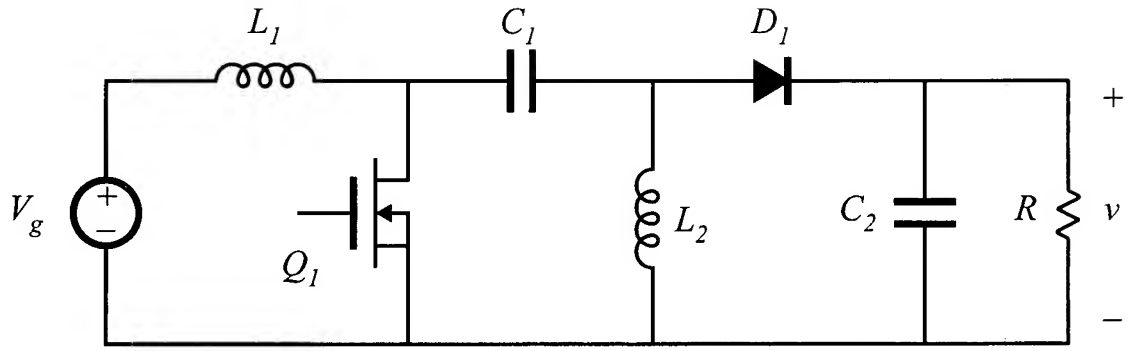
$$M(D) = \frac{V}{V_g} = \frac{n}{D'}$$

Push-pull converter based on Watkins-Johnson converter

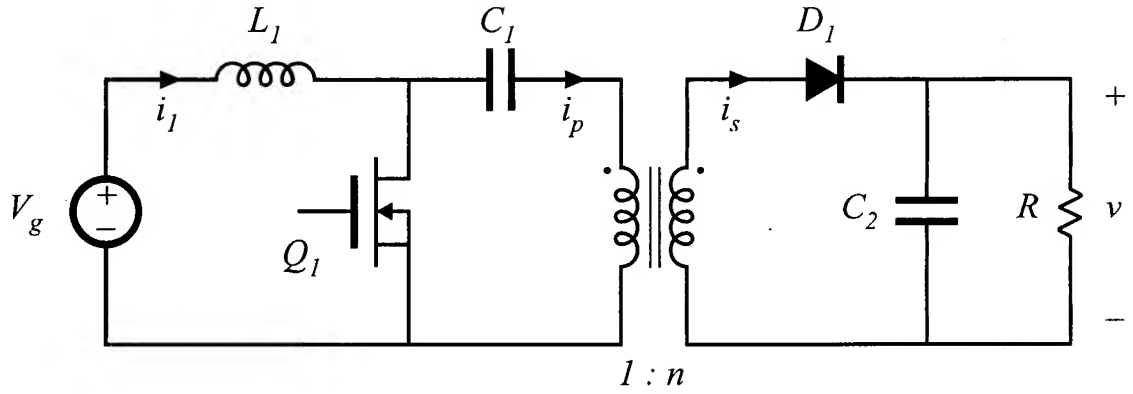


6.3.6. Isolated versions of the SEPIC and Cuk converter

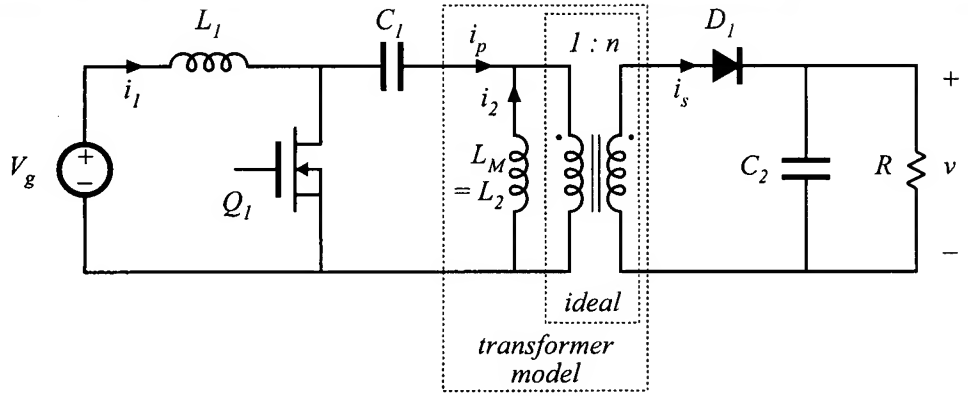
Basic nonisolated SEPIC

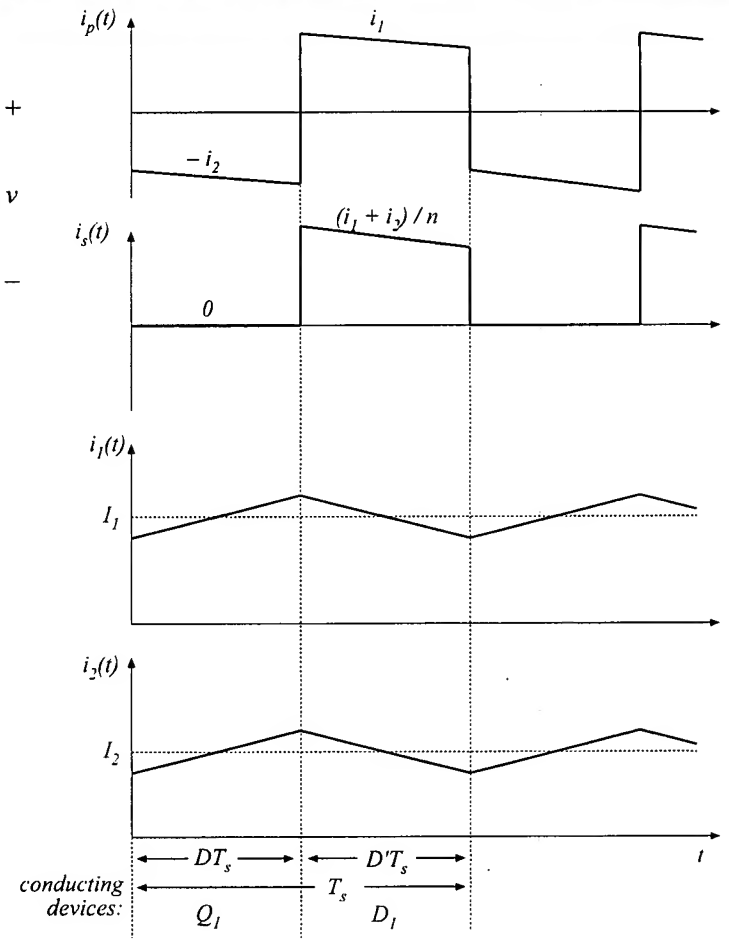


Isolated SEPIC



Isolated SEPIC

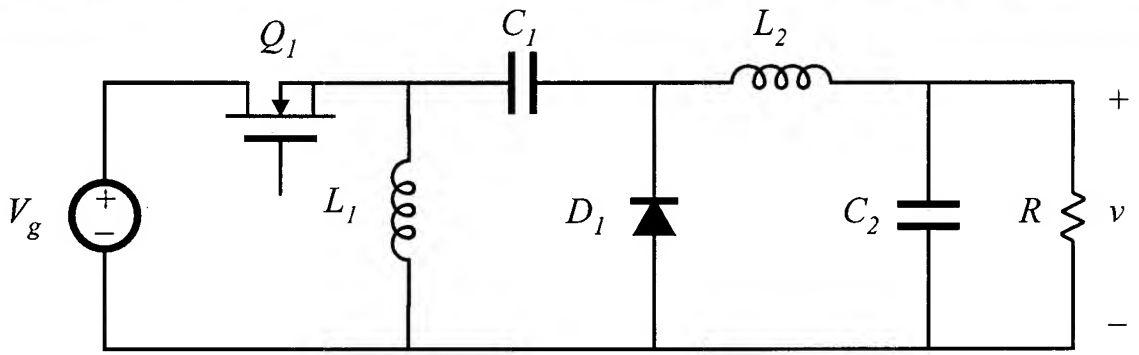




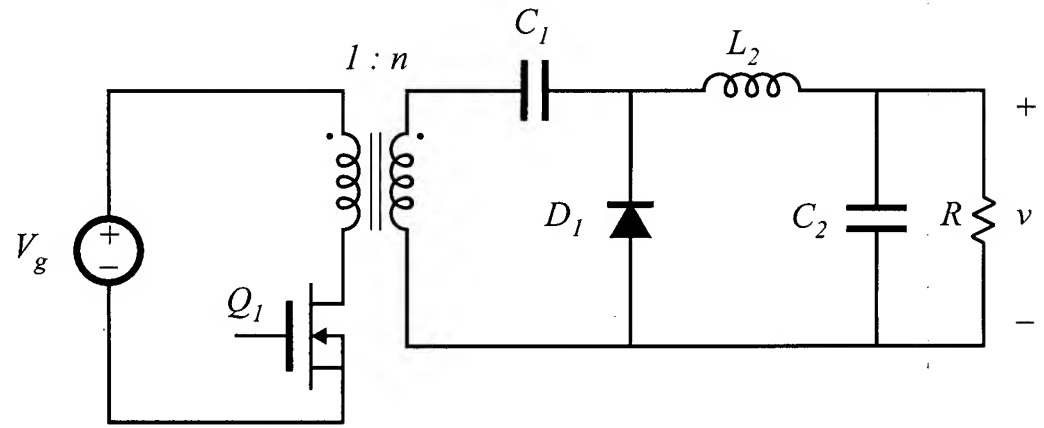
$$M(D) = \frac{V}{V_g} = \frac{n\,D}{D'}$$

Inverse SEPIC

Nonisolated inverse SEPIC

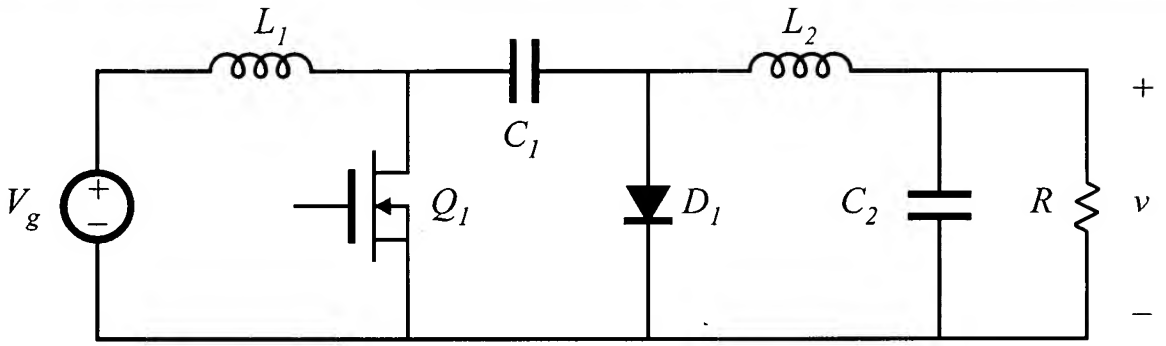


Isolated inverse SEPIC

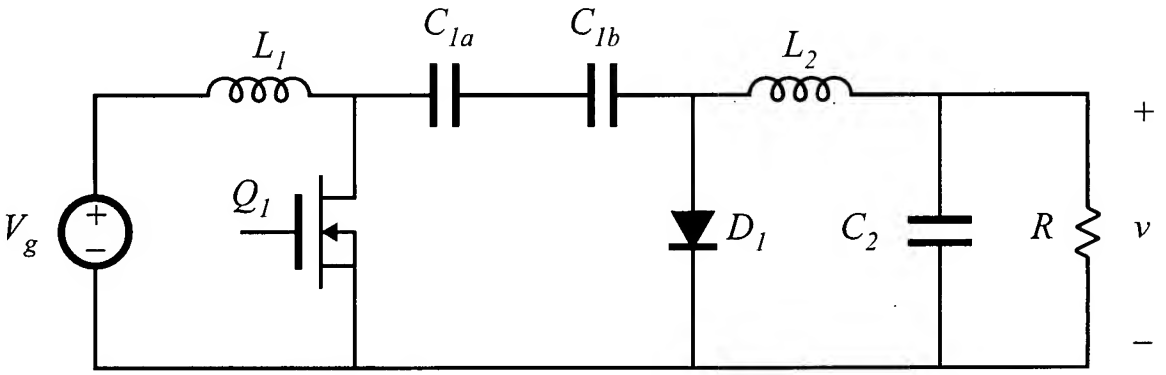


Obtaining isolation in the Cuk converter

Nonisolated Cuk converter



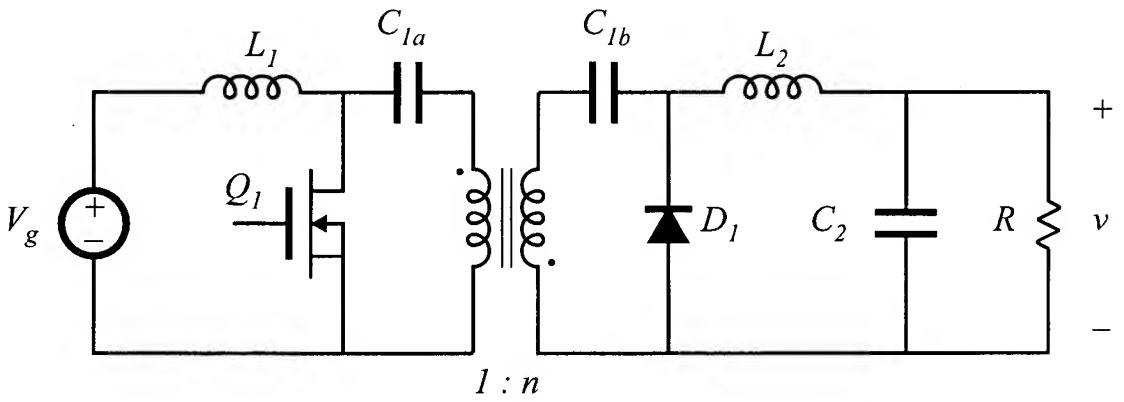
Split capacitor C_1 into series capacitors C_{1a} and C_{1b}



Isolated Cuk converter

Insert transformer between capacitors C_{1a} and C_{1b}

$$M(D) = \frac{V}{V_g} = \frac{n\,D}{D'}$$



Discussion

- Capacitors C_{1a} and C_{1b} ensure that no dc voltage is applied to transformer primary or secondary windings
- Transformer functions in conventional manner, with small magnetizing current and negligible energy storage within the magnetizing inductance

6.4. Converter evaluation and design

For a given application, which converter topology is best?

There is no ultimate converter, perfectly suited for all possible applications

Trade studies

- Rough designs of several converter topologies to meet the given specifications
- An unbiased quantitative comparison of worst-case transistor currents and voltages, transformer size, etc.

Comparison via switch stress, switch utilization, and semiconductor cost

Spreadsheet design

6.4.1. Switch stress and switch utilization

- Largest single cost in a converter is usually the cost of the active semiconductor devices
- Conduction and switching losses associated with the active semiconductor devices often dominate the other sources of loss

This suggests evaluating candidate converter approaches by comparing the voltage and current stresses imposed on the active semiconductor devices.

Minimization of total switch stresses leads to reduced loss, and to minimization of the total silicon area required to realize the power devices of the converter.

Total active switch stress S

In a converter having k active semiconductor devices, the total active switch stress S is defined as

$$S = \sum_{j=1}^{k} V_j I_j$$

where

V_j is the peak voltage applied to switch j,

I_j is the rms current applied to switch j (peak current is also sometimes used).

In a good design, the total active switch stress is minimized.

Active switch utilization U

It is desired to minimize the total active switch stress, while maximizing the output power P_{load}.

The active switch utilization U is defined as

$$U = \frac{P_{load}}{S}$$

The active switch utilization is the converter output power obtained per unit of active switch stress. It is a converter figure-of-merit, which measures how well a converter utilizes its semiconductor devices.

Active switch utilization is less than 1 in transformer-isolated converters, and is a quantity to be maximized.

Converters having low switch utilizations require extra active silicon area, and operate with relatively low efficiency.

Active switch utilization is a function of converter operating point.

CCM flyback example: Determination of S

During subinterval 2, the transistor blocks voltage $V_{Q1,pk}$ equal to V_g plus the reflected load voltage:

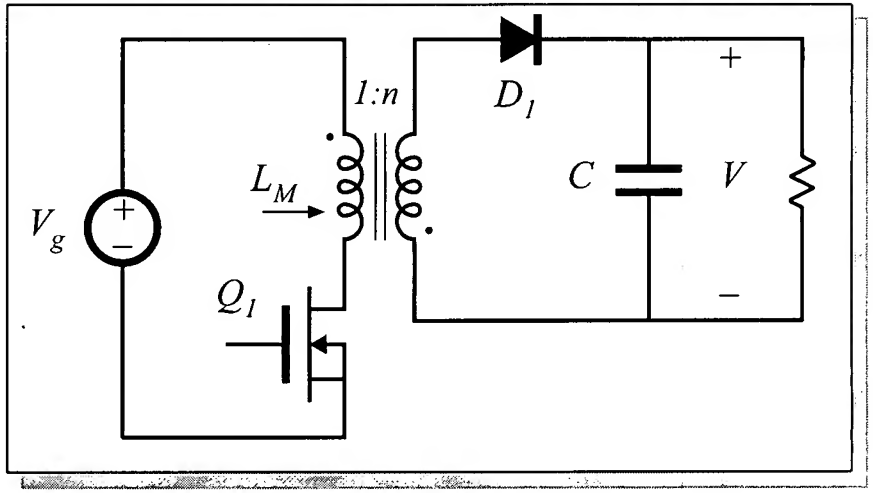
$$V_{Q1,pk} = V_g + V / n = \frac{V_g}{D'}$$

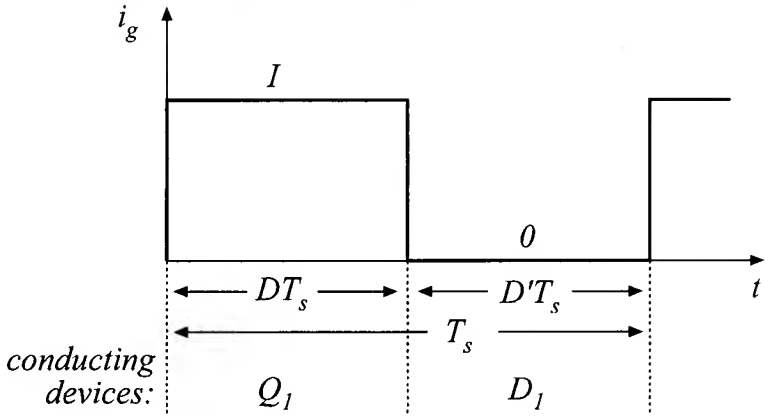
Transistor current coincides with $i_g(t)$. RMS value is

$$I_{Q1,rms} = I\sqrt{D} = \frac{P_{load}}{V_g\sqrt{D}}$$

Switch stress S is

$$S = V_{Q1,pk}\, I_{Q1,rms} = (V_g + V / n)\,(I\sqrt{D})$$

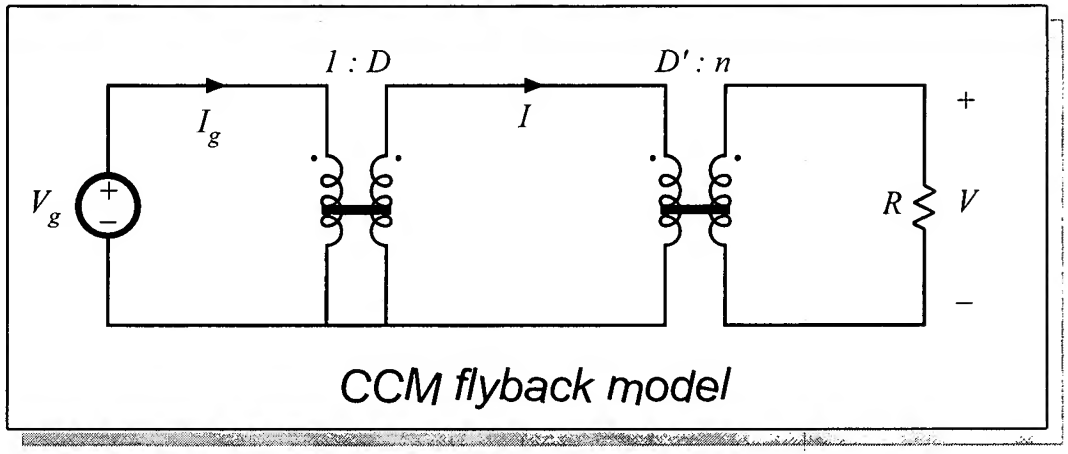




CCM flyback example: Determination of U

Express load power P_{load} in terms of V and I:

$$P_{load} = D' \, V \, \frac{I}{n}$$



CCM flyback model

Previously-derived expression for S:

$$S = V_{Q1,pk} \, I_{Q1,rms} = (V_g + V / n) \, (I \sqrt{D})$$

Hence switch utilization U is

$$U = \frac{P_{load}}{S} = D' \sqrt{D}$$

Flyback example: switch utilization $U(D)$

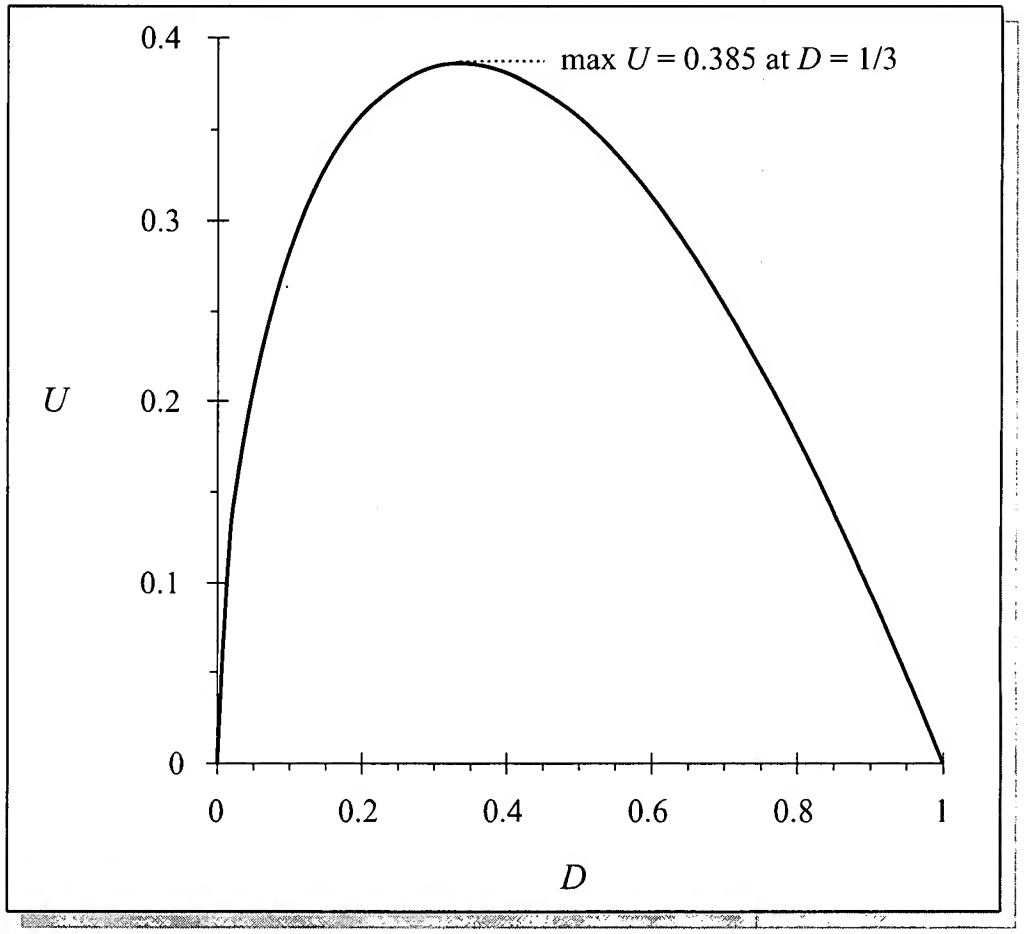
For given V, V_g, P_{load}, the designer can arbitrarily choose D. The turns ratio n must then be chosen according to

$$n = \frac{V}{V_g}\frac{D'}{D}$$

Single operating point design: choose $D = 1/3$.

small D leads to large transistor current

large D leads to large transistor voltage



Comparison of switch utilizations of some common converters

Table 6.1. Active switch utilizations of some common dc-dc converters, single operating point.

Converter	*U(D)*	max *U(D)*	max *U(D)* *occurs at D =*
Buck	$\sqrt{D}$	1	1
Boost	$\frac{D'}{\sqrt{D}}$	∞	0
Buck-boost, flyback, nonisolated SEPIC, isolated SEPIC, nonisolated Cuk, isolated Cuk	$D'\sqrt{D}$	$\frac{2}{3\sqrt{3}} = 0.385$	$\frac{1}{3}$
Forward, $n_1 = n_2$	$\frac{1}{2}\sqrt{D}$	$\frac{1}{2\sqrt{2}} = 0.353$	$\frac{1}{2}$
Other isolated buck-derived converters (full-bridge, half-bridge, push-pull)	$\frac{\sqrt{D}}{2\sqrt{2}}$	$\frac{1}{2\sqrt{2}} = 0.353$	1
Isolated boost-derived converters (full bridge, push-pull)	$\frac{D'}{2\sqrt{1+D}}$	$\frac{1}{2}$	0

Switch utilization : Discussion

- Increasing the range of operating points leads to reduced switch utilization
- Buck converter

  can operate with high switch utilization (U approaching 1) when D is close to 1
- Boost converter

  can operate with high switch utilization (U approaching ∞) when D is close to 1
- Transformer isolation leads to reduced switch utilization
- Buck-derived transformer-isolated converters

  $U \leq 0.353$

  should be designed to operate with D as large as other considerations allow

  transformer turns ratio can be chosen to optimize design

Switch utilization: Discussion

- Nonisolated and isolated versions of buck-boost, SEPIC, and Cuk converters
  - $U \leq 0.385$
  - Single-operating-point optimum occurs at $D = 1/3$
  - Nonisolated converters have lower switch utilizations than buck or boost
  - Isolation can be obtained without penalizing switch utilization

Active semiconductor cost vs. switch utilization

$$\left(\begin{array}{c}\textit{semiconductor cost}\\ \textit{per kW output power}\end{array}\right) = \frac{\left(\begin{array}{c}\textit{semiconductor device cost}\\ \textit{per rated kVA}\end{array}\right)}{\left(\begin{array}{c}\textit{voltage}\\ \textit{derating}\\ \textit{factor}\end{array}\right)\left(\begin{array}{c}\textit{current}\\ \textit{derating}\\ \textit{factor}\end{array}\right)\left(\begin{array}{c}\textit{converter}\\ \textit{switch}\\ \textit{utilization}\end{array}\right)}$$

(semiconductor device cost per rated kVA) = cost of device, divided by product of rated blocking voltage and rms current, in \$/kVA. Typical values are less than \$1/kVA

(voltage derating factor) and (current derating factor) are required to obtain reliable operation. Typical derating factors are 0.5 - 0.75

Typical cost of active semiconductor devices in an isolated dc-dc converter: \$1 - \$10 per kW of output power.

6.4.2. Converter design using computer spreadsheet

Given ranges of V_g and P_{load}, as well as desired value of V and other quantities such as switching frequency, ripple, etc., there are two basic engineering design tasks:

- Compare converter topologies and select the best for the given specifications
- Optimize the design of a given converter

A computer spreadsheet is a very useful tool for this job. The results of the steady-state converter analyses of chapters 1-6 can be entered, and detailed design investigations can be quickly performed:

- Evaluation of worst-case stresses over a range of operating points
- Evaluation of design tradeoffs

Spreadsheet design example

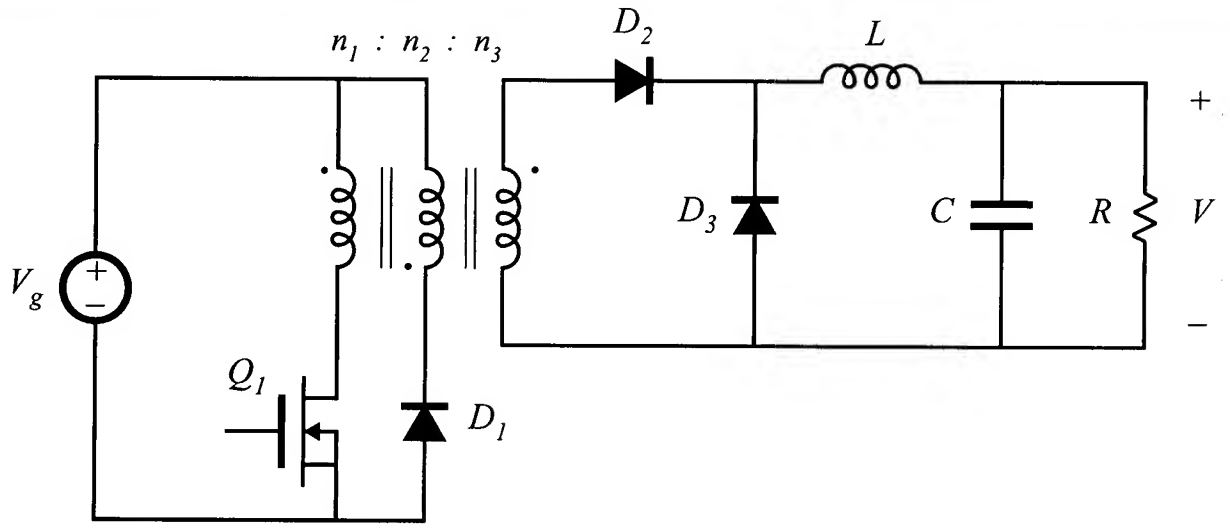
Specifications	
maximum input voltage V_g	390V
minimum input voltage V_g	260V
output voltage V	15V
maximum load power P_{load}	200W
minimum load power P_{load}	20W
switching frequency f_s	100kHz
maximum output ripple Δv	0.1V

- Input voltage: rectified 230Vrms ±20%
- Regulated output of 15V
- Rated load power 200W
- Must operate at 10% load
- Select switching frequency of 100kHz
- Output voltage ripple ≤ 0.1V

Compare single-transistor forward and flyback converters in this application

Specifications are entered at top of spreadsheet

Forward converter design, CCM

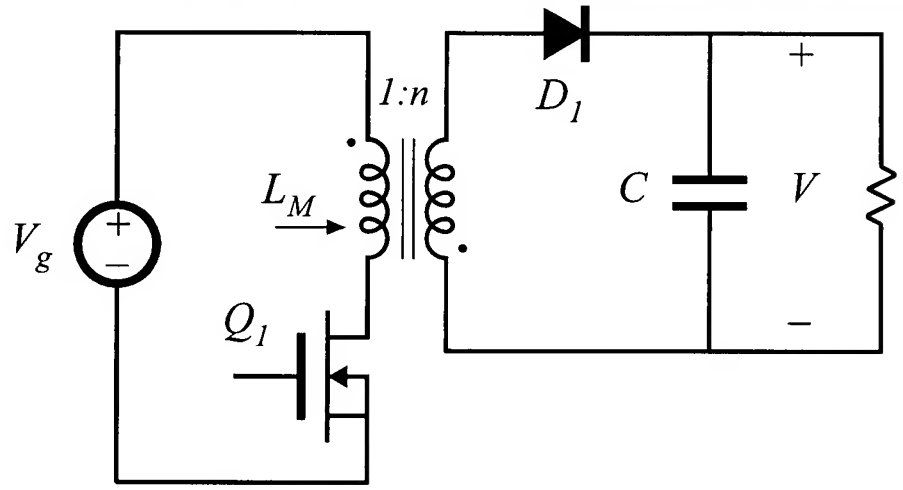


Design variables

reset winding turns ratio n_2 / n_1	1
turns ratio n_3 / n_1	0.125
inductor current ripple Δi	2A ref to sec

- Design for CCM at full load; may operate in DCM at light load

Flyback converter design, CCM



Design variables

turns ratio n_2 / n_1	0.125
inductor current ripple Δi	3A ref to sec

- Design for CCM at full load; may operate in DCM at light load

Enter results of converter analysis into spreadsheet (Forward converter example)

Maximum duty cycle occurs at minimum V_g and maximum P_{load}. Converter then operates in CCM, with

$$D = \frac{n_1}{n_3} \frac{V}{V_g}$$

Inductor current ripple is

$$\Delta i = \frac{D' V T_s}{2 L}$$

Solve for L:

$$L = \frac{D' V T_s}{2 \Delta i}$$

Δi is a design variable. For a given Δi, the equation above can be used to determine L. To ensure CCM operation at full load, Δi should be less than the full-load output current. C can be found in a similar manner.

Forward converter example, continued

Check for DCM at light load. The solution of the buck converter operating in DCM is

$$V = \frac{n_3}{n_1} V_g \frac{2}{\sqrt{1 + 4K / D^2}}$$

with $K = 2 L / R T_s$, and $R = V^2 / P_{load}$

These equations apply equally well to the forward converter, provided that all quantities are referred to the transformer secondary side.

Solve for D:

$$D = \frac{2\sqrt{K}}{\sqrt{\left(\frac{2 n_3 V_g}{n_1 V} - 1\right)^2 - 1}} \quad \text{in DCM} \qquad D = \frac{n_1}{n_3} \frac{V}{V_g} \quad \text{in CCM}$$

at a given operating point, the actual duty cycle is the small of the values calculated by the CCM and DCM equations above. Minimum D occurs at minimum P_{load} and maximum V_g.

More regarding forward converter example

Worst-case component stresses can now be evaluated.

Peak transistor voltage is

$$\max v_{Q1} = V_g \left(1 + \frac{n_1}{n_2} \right)$$

Rms transistor current is

$$I_{Q1,\,rms} = \frac{n_3}{n_1} \sqrt{D} \sqrt{I^2 + (\Delta i)^2 / 3} \approx \frac{n_3}{n_1} \sqrt{D}\, I$$

(this neglects transformer magnetizing current)

Other component stresses can be found in a similar manner.
Magnetics design is left for a later chapter.

Results: forward and flyback converter spreadsheets

Forward converter design, CCM	
Design variables	
reset winding turns ratio n_2 / n_1	1
turns ratio n_3 / n_1	0.125
inductor current ripple Δi	2A ref to sec
Results	
maximum duty cycle D	0.462
minimum D, at full load	0.308
minimum D, at minimum load	0.251
Worst-case stresses	
peak transistor voltage v_{Q1}	780V
rms transistor current i_{Q1}	1.13A
transistor utilization U	0.226
peak diode voltage v_{D1}	49V
rms diode current i_{D1}	9.1A
peak diode voltage v_{D2}	49V
rms diode current i_{D2}	11.1A
rms output capacitor current i_C	1.15A

Flyback converter design, CCM	
Design variables	
turns ratio n_2 / n_1	0.125
inductor current ripple Δi	3A ref to sec
Results	
maximum duty cycle D	0.316
minimum D, at full load	0.235
minimum D, at minimum load	0.179
Worst-case stresses	
peak transistor voltage v_{Q1}	510V
rms transistor current i_{Q1}	1.38A
transistor utilization U	0.284
peak diode voltage v_{D1}	64V
rms diode current i_{D1}	16.3A
peak diode current i_{D1}	22.2A
rms output capacitor current i_C	9.1A

Discussion: transistor voltage

Flyback converter

Ideal peak transistor voltage: 510V

Actual peak voltage will be higher, due to ringing causes by transformer leakage inductance

An 800V or 1000V MOSFET would have an adequate design margin

Forward converter

Ideal peak transistor voltage: 780V, 53% greater than flyback

MOSFETs having voltage rating greater than 1000V are not available (in 1995) —when ringing due to transformer leakage inductance is accounted for, this design will have an inadequate design margin

Fix: use two-transistor forward converter, or change reset winding turns ratio

A conclusion: reset mechanism of flyback is superior to forward

Discussion: rms transistor current

Forward

1.13A worst-case

transistor utilization 0.226

Flyback

1.38A worst case, 22% higher than forward

transistor utilization 0.284

CCM flyback exhibits higher peak and rms currents. Currents in DCM flyback are even higher

Discussion: secondary-side diode and capacitor stresses

Forward

peak diode voltage 49V

rms diode current 9.1A / 11.1A

rms capacitor current 1.15A

Flyback

peak diode voltage 64V

rms diode current 16.3A

peak diode current 22.2A

rms capacitor current 9.1A

Secondary-side currents, especially capacitor currents, limit the practical application of the flyback converter to situations where the load current is not too great.

Summary of key points

1. The boost converter can be viewed as an inverse buck converter, while the buck-boost and Cuk converters arise from cascade connections of buck and boost converters. The properties of these converters are consistent with their origins. Ac outputs can be obtained by differential connection of the load. An infinite number of converters are possible, and several are listed in this chapter.
2. For understanding the operation of most converters containing transformers, the transformer can be modeled as a magnetizing inductance in parallel with an ideal transformer. The magnetizing inductance must obey all of the usual rules for inductors, including the principle of volt-second balance.

Summary of key points

3. The steady-state behavior of transformer-isolated converters may be understood by first replacing the transformer with the magnetizing-inductance-plus-ideal-transformer equivalent circuit. The techniques developed in the previous chapters can then be applied, including use of inductor volt-second balance and capacitor charge balance to find dc currents and voltages, use of equivalent circuits to model losses and efficiency, and analysis of the discontinuous conduction mode.
4. In the full-bridge, half-bridge, and push-pull isolated versions of the buck and/or boost converters, the transformer frequency is twice the output ripple frequency. The transformer is reset while it transfers energy: the applied voltage polarity alternates on successive switching periods.

Summary of key points

5. In the conventional forward converter, the transformer is reset while the transistor is off. The transformer magnetizing inductance operates in the discontinuous conduction mode, and the maximum duty cycle is limited.
6. The flyback converter is based on the buck-boost converter. The flyback transformer is actually a two-winding inductor, which stores and transfers energy.
7. The transformer turns ratio is an extra degree-of-freedom which the designer can choose to optimize the converter design. Use of a computer spreadsheet is an effective way to determine how the choice of turns ratio affects the component voltage and current stresses.
8. Total active switch stress, and active switch utilization, are two simplified figures-of-merit which can be used to compare the various converter circuits.

Chapter 19

Resonant Conversion

Introduction to Resonant Conversion

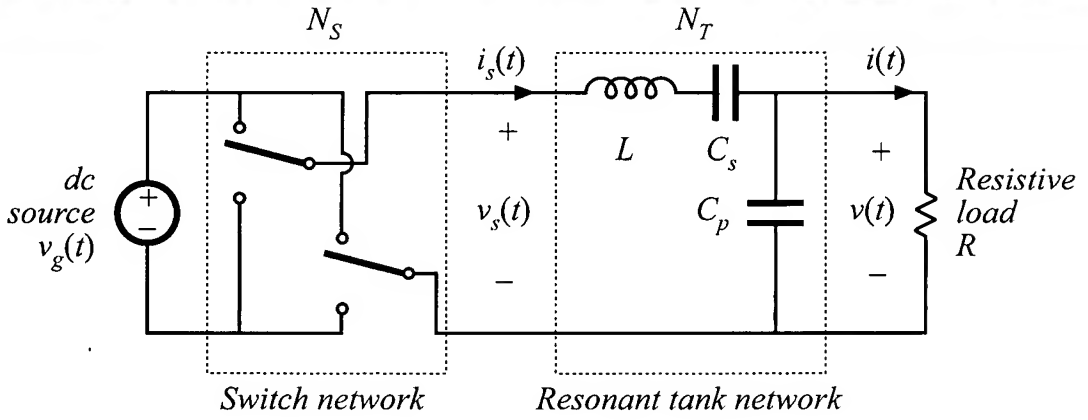
Resonant power converters contain resonant L-C networks whose voltage and current waveforms vary sinusoidally during one or more subintervals of each switching period. These sinusoidal variations are large in magnitude, and the small ripple approximation does not apply.

Some types of resonant converters:

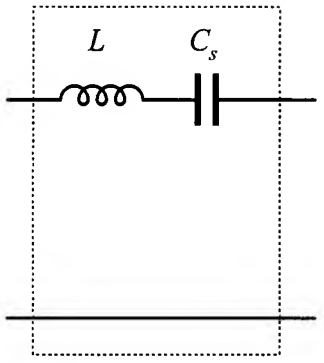
- Dc-to-high-frequency-ac inverters
- Resonant dc-dc converters
- Resonant inverters or rectifiers producing line-frequency ac

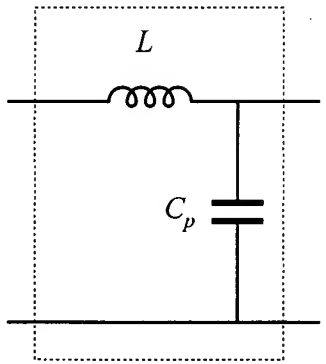
A basic class of resonant inverters

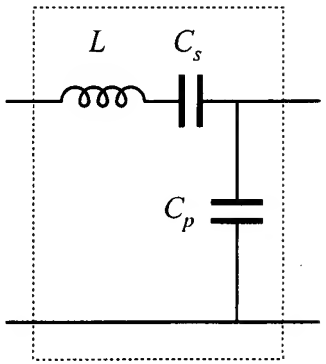
Basic circuit



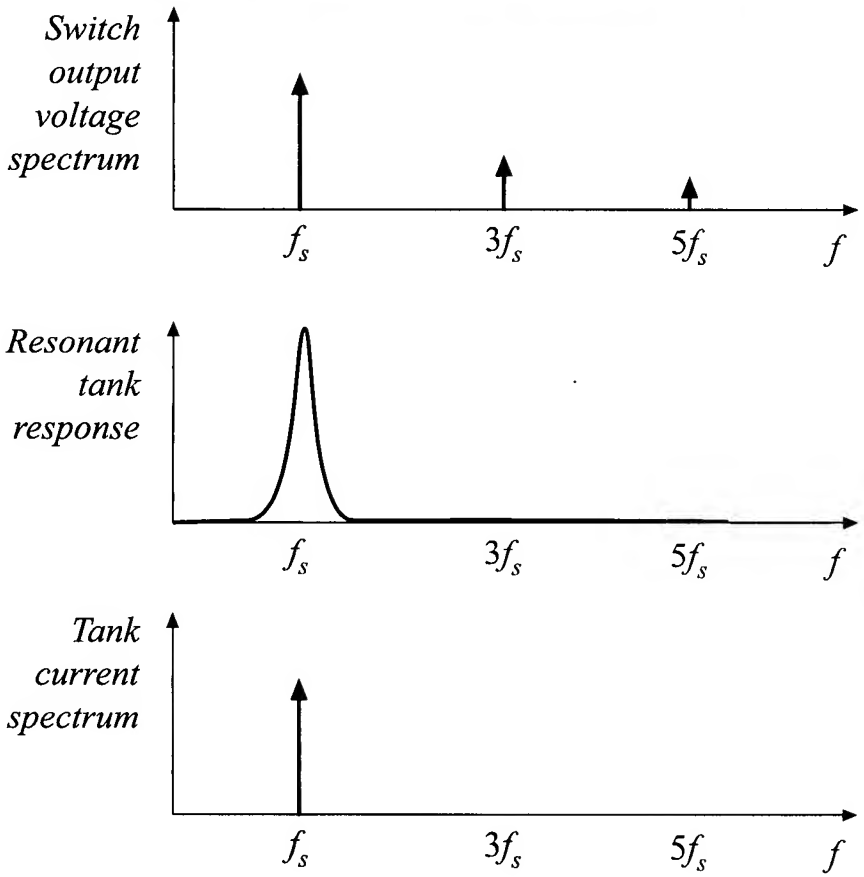
Several resonant tank networks







Tank network responds only to fundamental component of switched waveforms

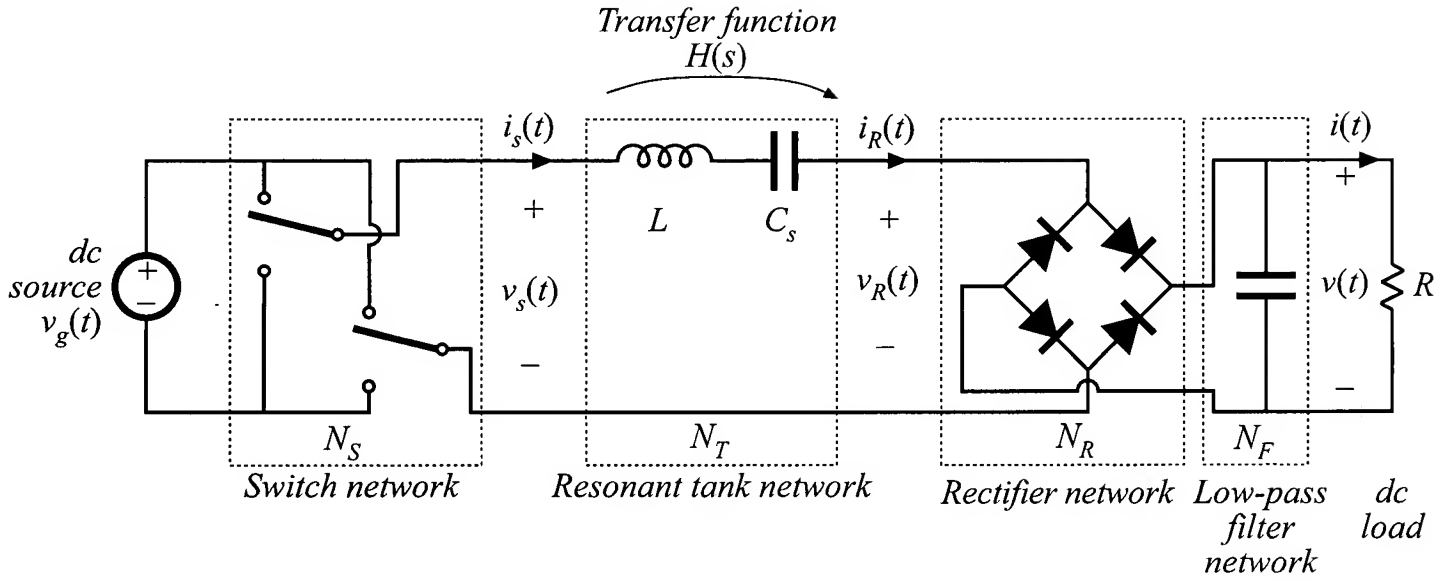


Tank current and output voltage are essentially sinusoids at the switching frequency f_s.

Output can be controlled by variation of switching frequency, closer to or away from the tank resonant frequency

Derivation of a resonant dc-dc converter

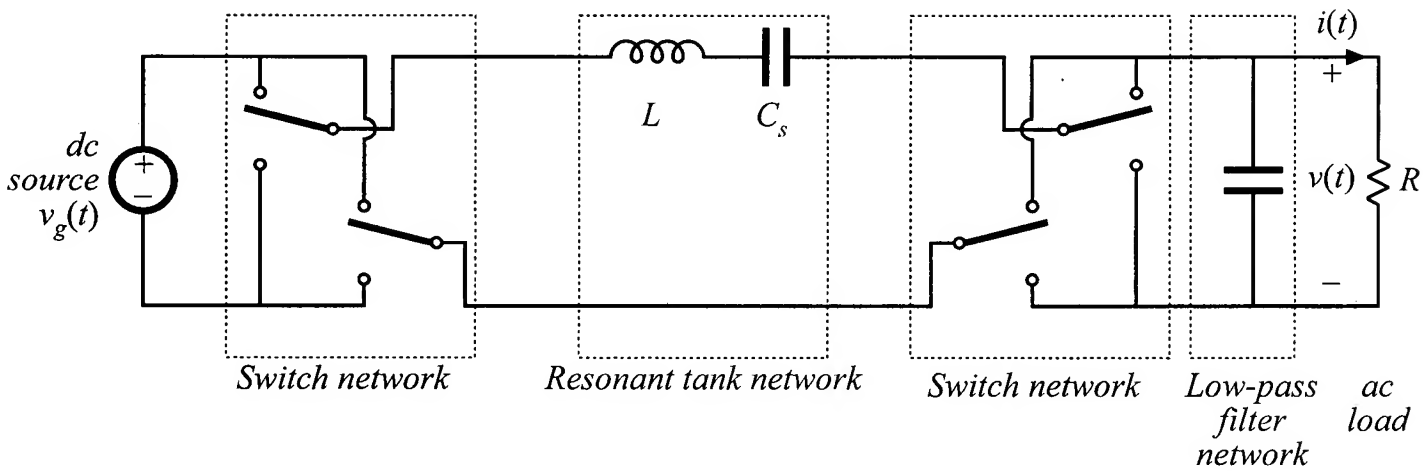
Rectify and filter the output of a dc-high-frequency-ac inverter



The series resonant dc-dc converter

A series resonant link inverter

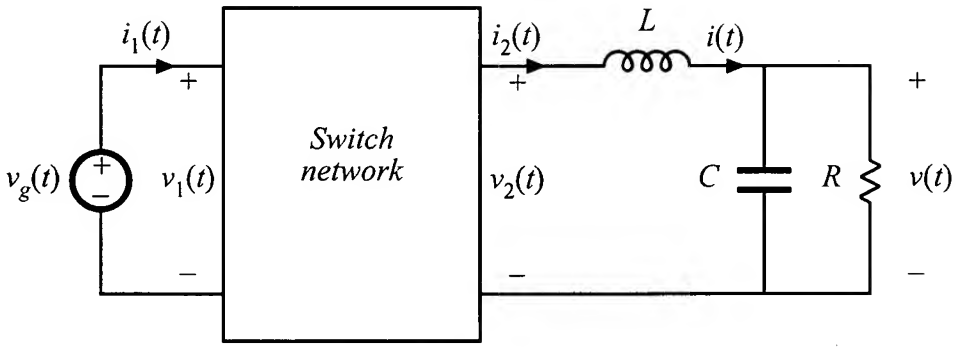
Same as dc-dc series resonant converter, except output rectifiers are replaced with four-quadrant switches:



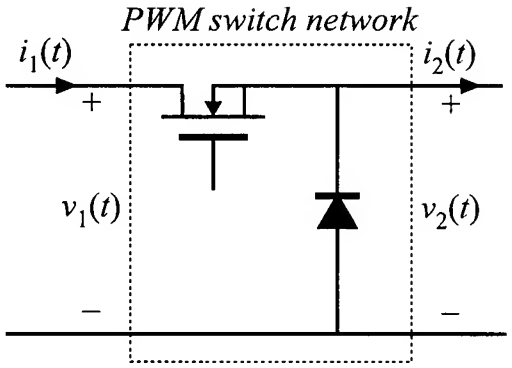
Quasi-resonant converters

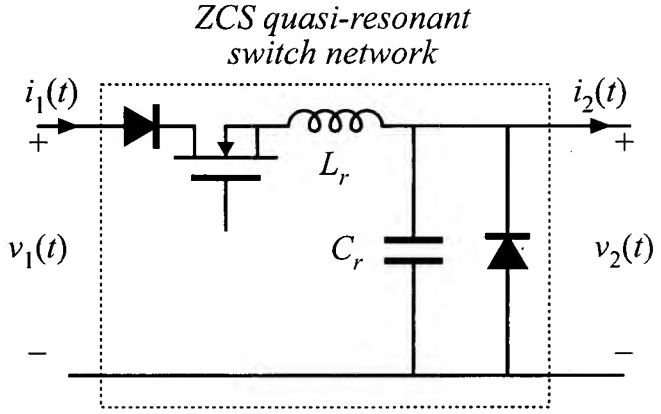
In a conventional PWM converter, replace the PWM switch network with a switch network containing resonant elements.

Buck converter example



Two switch networks:





Resonant conversion: advantages

The chief advantage of resonant converters: reduced switching loss

Zero-current switching

Zero-voltage switching

Turn-on or turn-off transitions of semiconductor devices can occur at zero crossings of tank voltage or current waveforms, thereby reducing or eliminating some of the switching loss mechanisms. Hence resonant converters can operate at higher switching frequencies than comparable PWM converters

Zero-voltage switching also reduces converter-generated EMI

Zero-current switching can be used to commutate SCRs

In specialized applications, resonant networks may be unavoidable

High voltage converters: significant transformer leakage inductance and winding capacitance leads to resonant network

Resonant conversion: disadvantages

Can optimize performance at one operating point, but not with wide range of input voltage and load power variations

Significant currents may circulate through the tank elements, even when the load is disconnected, leading to poor efficiency at light load

Quasi-sinusoidal waveforms exhibit higher peak values than equivalent rectangular waveforms

These considerations lead to increased conduction losses, which can offset the reduction in switching loss

Resonant converters are usually controlled by variation of switching frequency. In some schemes, the range of switching frequencies can be very large

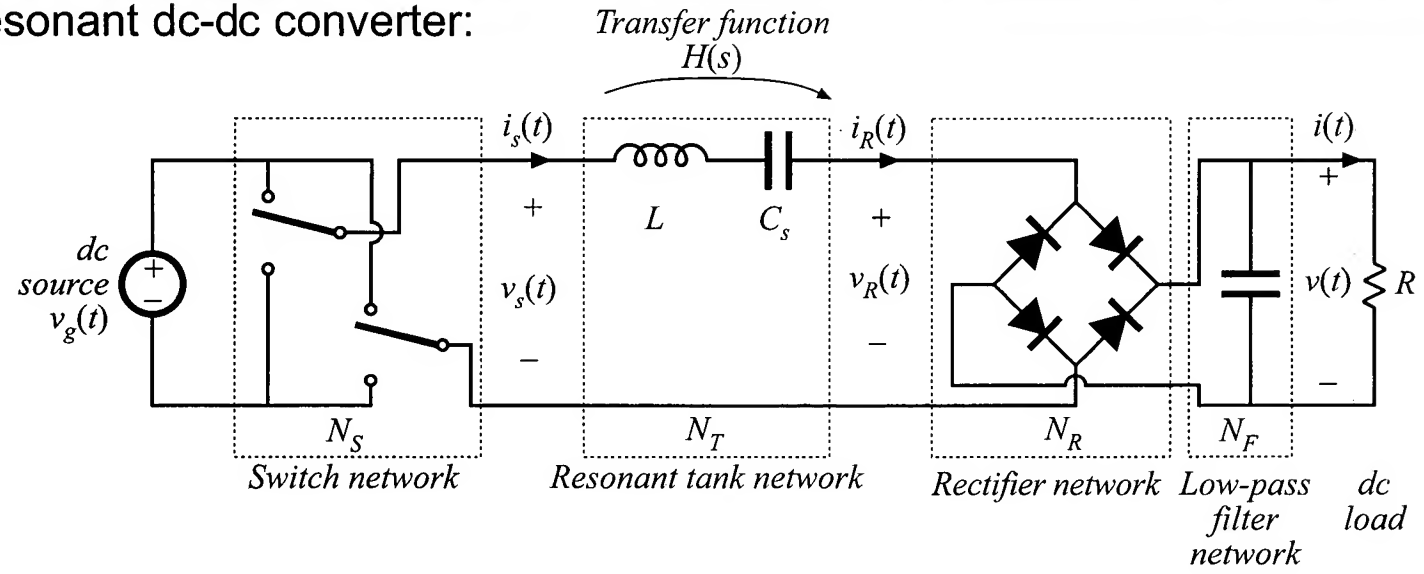
Complexity of analysis

Resonant conversion: Outline of discussion

- Simple steady-state analysis via sinusoidal approximation
- Simple and exact results for the series and parallel resonant converters
- Mechanisms of soft switching
- Circulating currents, and the dependence (or lack thereof) of conduction loss on load power
- Quasi-resonant converter topologies
- Steady-state analysis of quasi-resonant converters
- Ac modeling of quasi-resonant converters via averaged switch modeling

19.1 Sinusoidal analysis of resonant converters

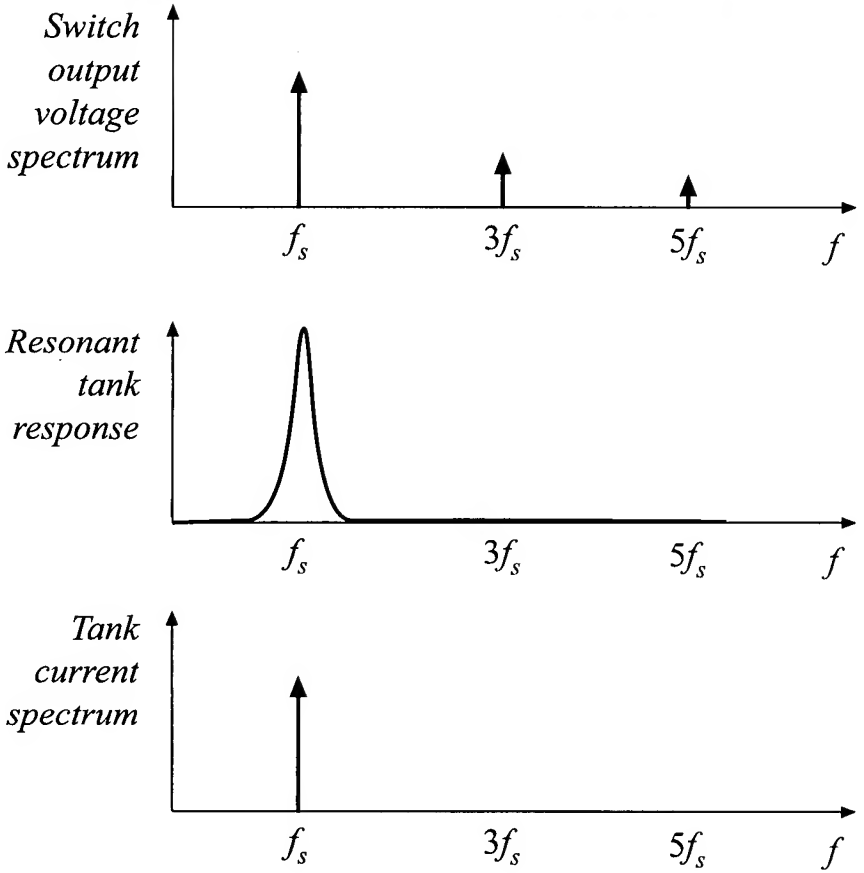
A resonant dc-dc converter:



If tank responds primarily to fundamental component of switch network output voltage waveform, then harmonics can be neglected.

Let us model all ac waveforms by their fundamental components.

The sinusoidal approximation

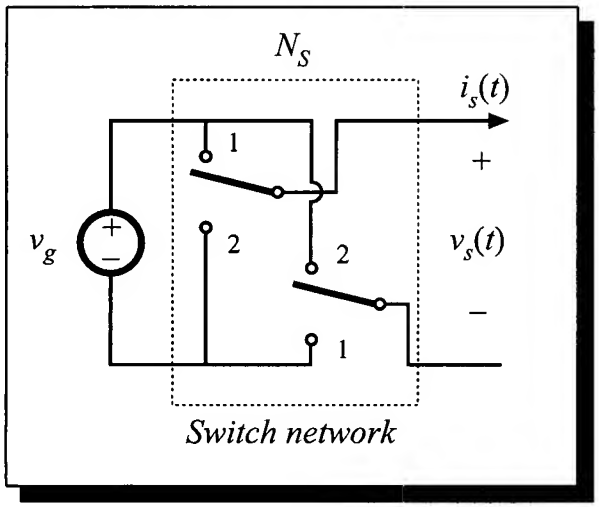


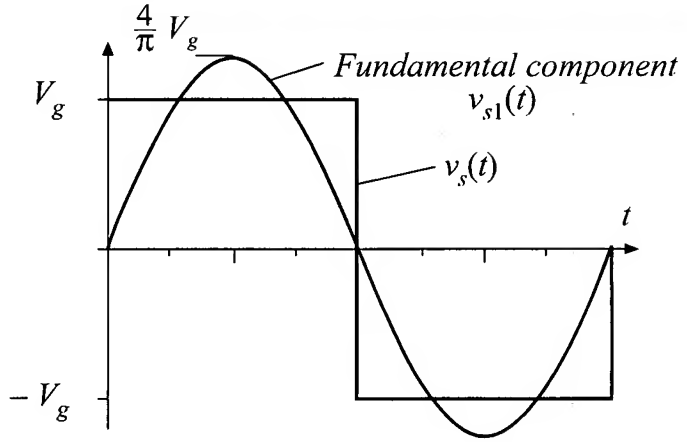
Tank current and output voltage are essentially sinusoids at the switching frequency f_s.

Neglect harmonics of switch output voltage waveform, and model only the fundamental component.

Remaining ac waveforms can be found via phasor analysis.

19.1.1 Controlled switch network model





If the switch network produces a square wave, then its output voltage has the following Fourier series:

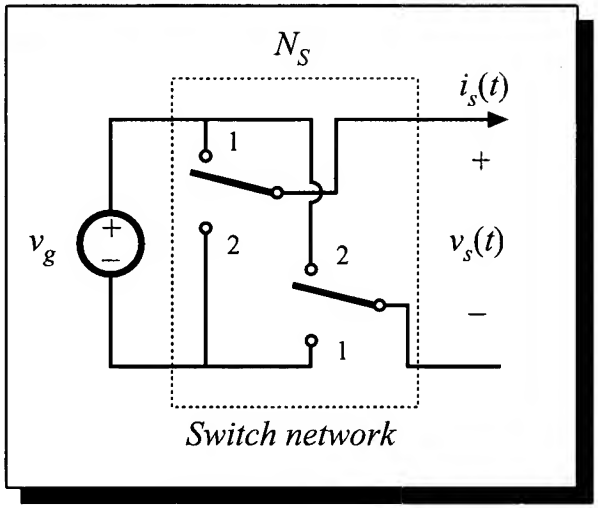
$$v_s(t) = \frac{4V_g}{\pi} \sum_{n=1,3,5,\ldots} \frac{1}{n} \sin(n\omega_s t)$$

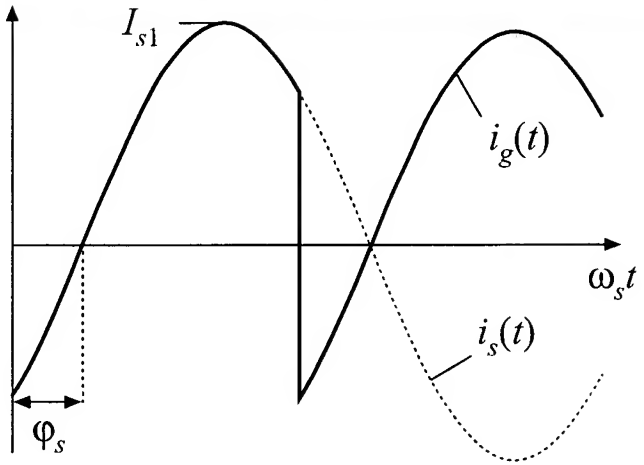
The fundamental component is

$$v_{s1}(t) = \frac{4V_g}{\pi} \sin(\omega_s t) = V_{s1} \sin(\omega_s t)$$

So model switch network output port with voltage source of value $v_{s1}(t)$

Model of switch network input port





Assume that switch network output current is

$$i_s(t) \approx I_{s1} \sin(\omega_s t - \varphi_s)$$

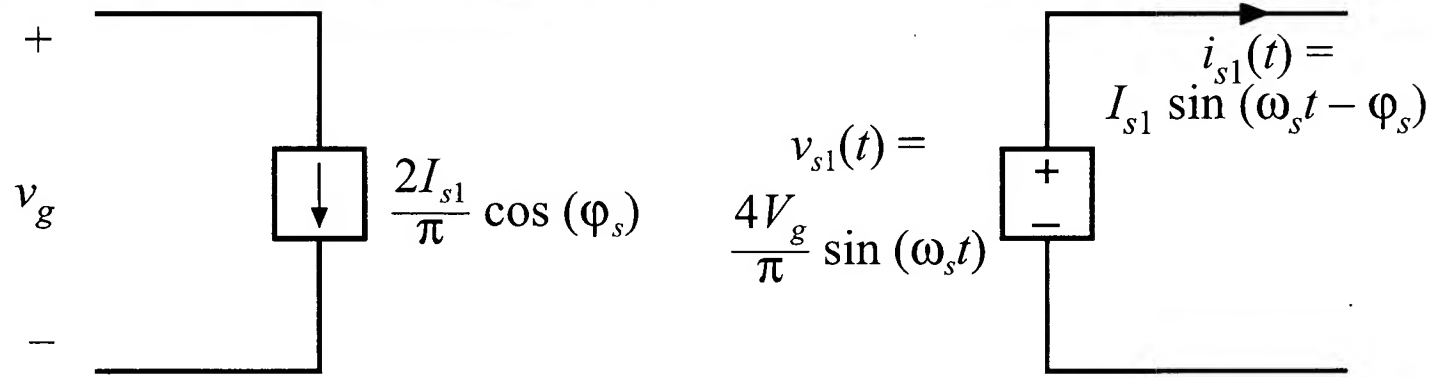
It is desired to model the dc component (average value) of the switch network input current.

$$\left\langle i_g(t) \right\rangle_{T_s} = \frac{2}{T_s} \int_0^{T_s/2} i_g(\tau) d\tau$$

$$\approx \frac{2}{T_s} \int_0^{T_s/2} I_{s1} \sin(\omega_s \tau - \varphi_s) d\tau$$

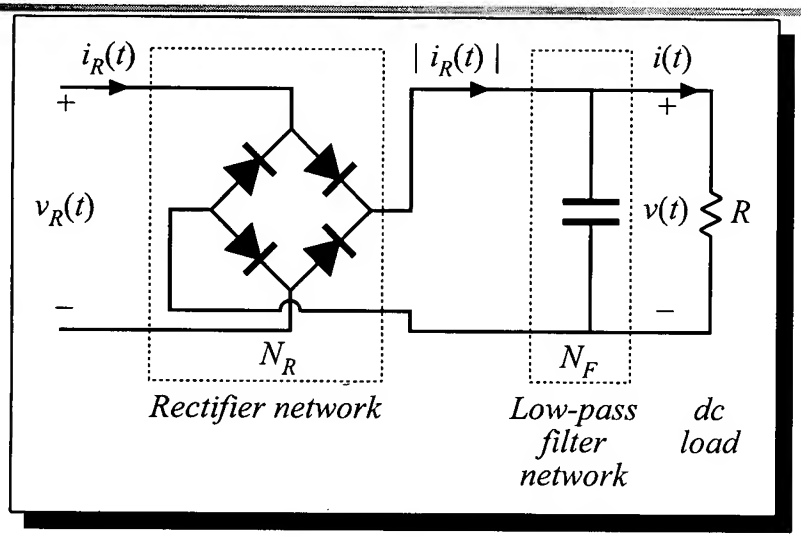
$$= \frac{2}{\pi} I_{s1} \cos(\varphi_s)$$

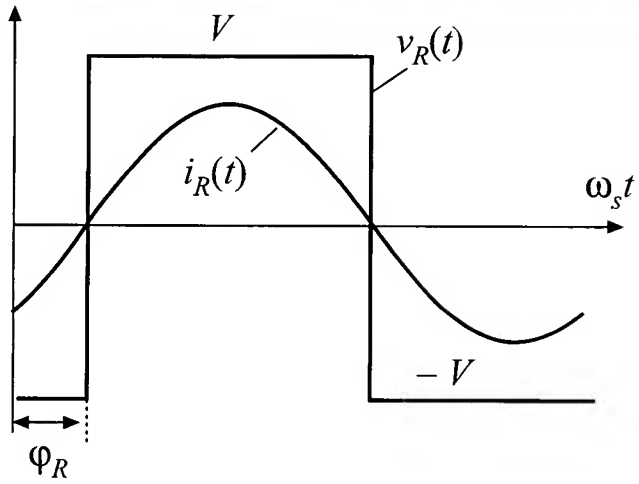
Switch network: equivalent circuit



- Switch network converts dc to ac
- Dc components of input port waveforms are modeled
- Fundamental ac components of output port waveforms are modeled
- Model is power conservative: predicted average input and output powers are equal

19.1.2 Modeling the rectifier and capacitive filter networks





Assume large output filter capacitor, having small ripple.

$v_R(t)$ is a square wave, having zero crossings in phase with tank output current $i_R(t)$.

If $i_R(t)$ is a sinusoid:

$$i_R(t) = I_{R1} \sin(\omega_s t - \varphi_R)$$

Then $v_R(t)$ has the following Fourier series:

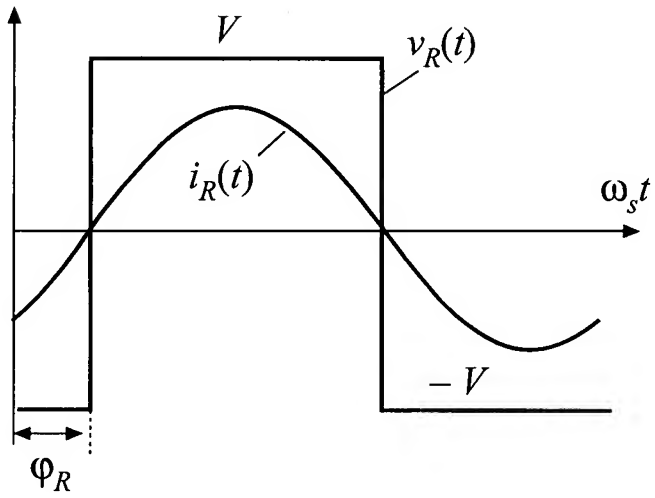
$$v_R(t) = \frac{4V}{\pi} \sum_{n=1,3,5,\cdots}^{\infty} \frac{1}{n} \sin(n\omega_s t - \varphi_R)$$

Sinusoidal approximation: rectifier

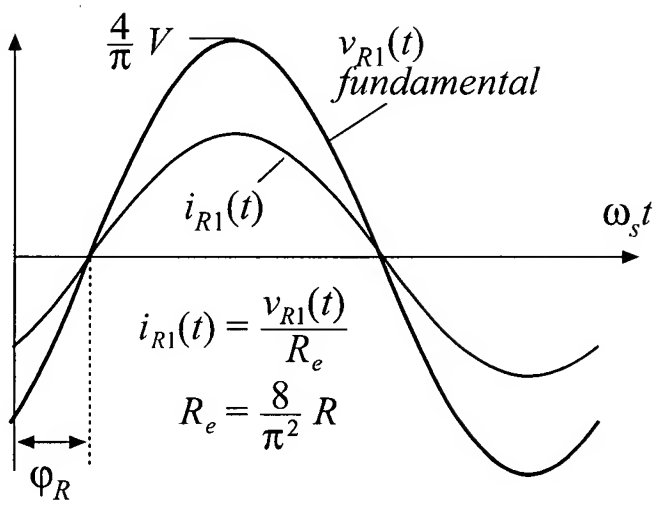
Again, since tank responds only to fundamental components of applied waveforms, harmonics in $v_R(t)$ can be neglected. $v_R(t)$ becomes

$$v_{R1}(t) = \frac{4V}{\pi} \sin(\omega_s t - \varphi_R) = V_{R1} \sin(\omega_s t - \varphi_R)$$

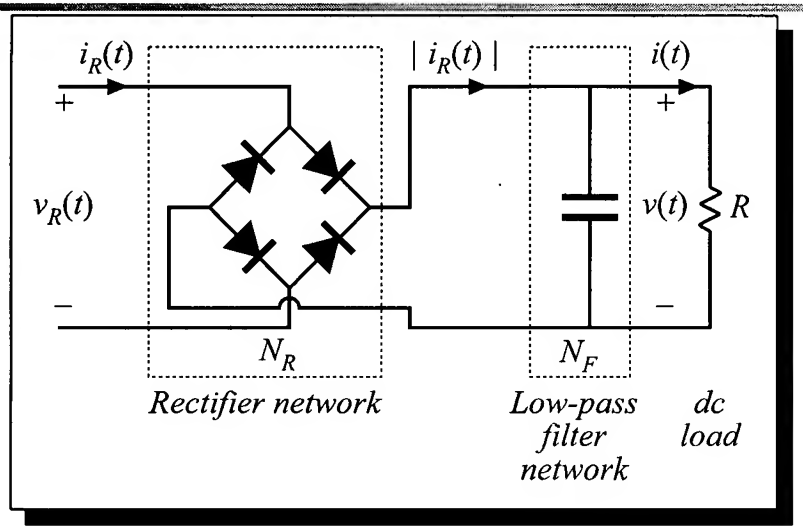
Actual waveforms

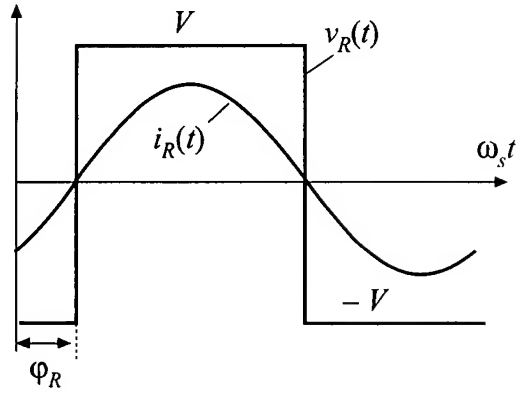


with harmonics ignored



Rectifier dc output port model





Output capacitor charge balance: dc load current is equal to average rectified tank output current

$$\left\langle \left| i_R(t) \right| \right\rangle_{T_s} = I$$

Hence

$$I = \frac{2}{T_S} \int_0^{T_s/2} I_{R1} \left| \sin\left(\omega_s t - \varphi_R\right) \right| dt$$

$$= \frac{2}{\pi} I_{R1}$$

Equivalent circuit of rectifier

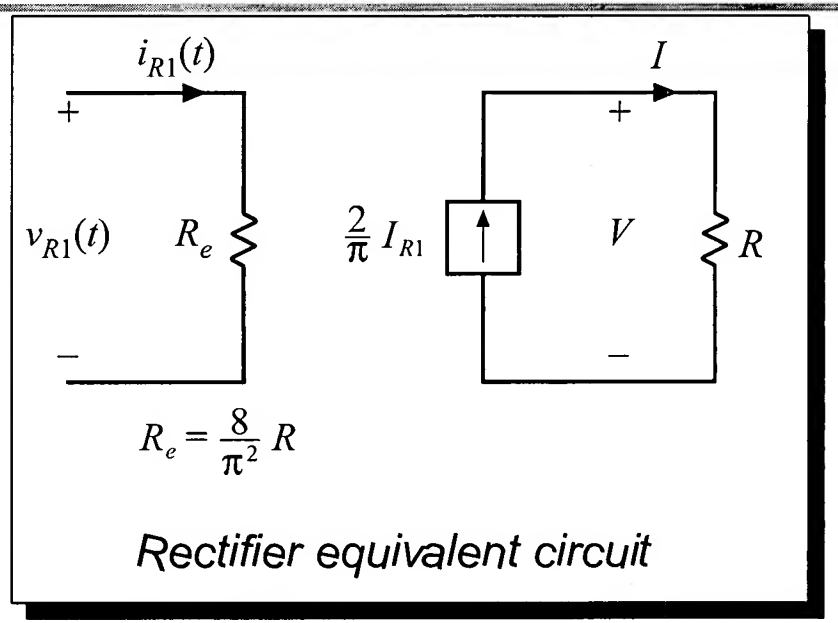
Rectifier input port:

Fundamental components of current and voltage are sinusoids that are in phase

Hence rectifier presents a resistive load to tank network

Effective resistance R_e is

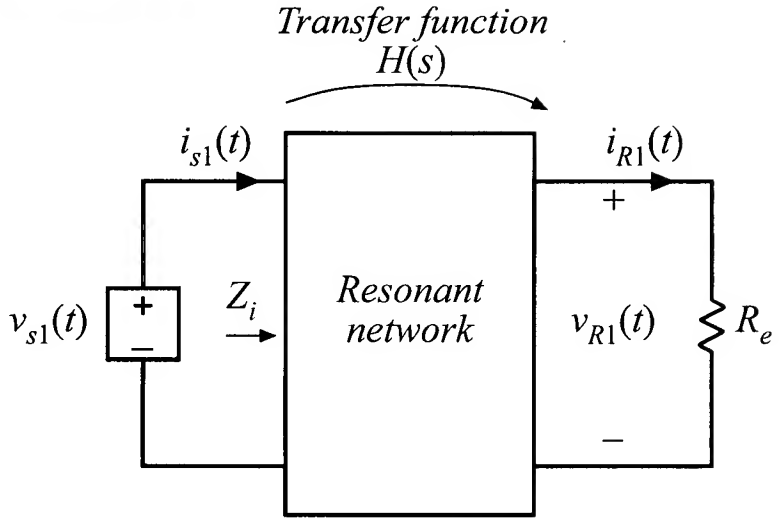
$$R_e = \frac{v_{R1}(t)}{i_R(t)} = \frac{8}{\pi^2}\frac{V}{I}$$



With a resistive load R, this becomes

$$R_e = \frac{8}{\pi^2} R = 0.8106R$$

19.1.3 Resonant tank network



Model of ac waveforms is now reduced to a linear circuit. Tank network is excited by effective sinusoidal voltage (switch network output port), and is load by effective resistive load (rectifier input port).

Can solve for transfer function via conventional linear circuit analysis.

Solution of tank network waveforms

Transfer function:

$$\frac{v_{R1}(s)}{v_{s1}(s)} = H(s)$$

Ratio of peak values of input and output voltages:

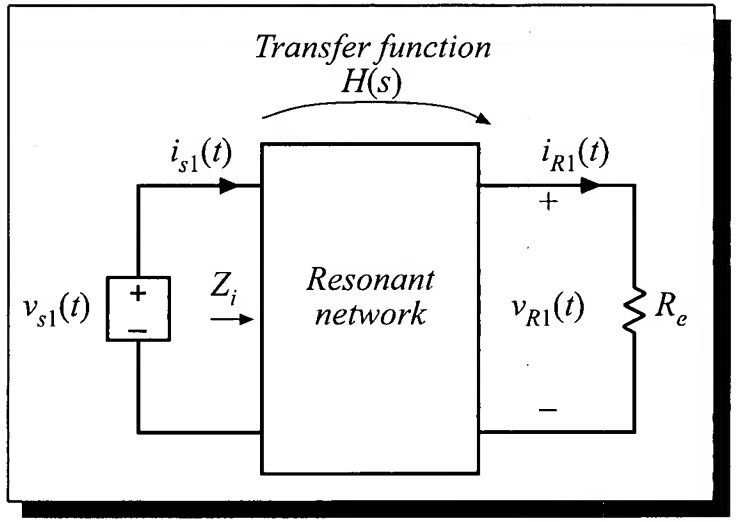
$$\frac{V_{R1}}{V_{s1}} = \left\| H(s) \right\|_{s = j\omega_s}$$

Solution for tank output current:

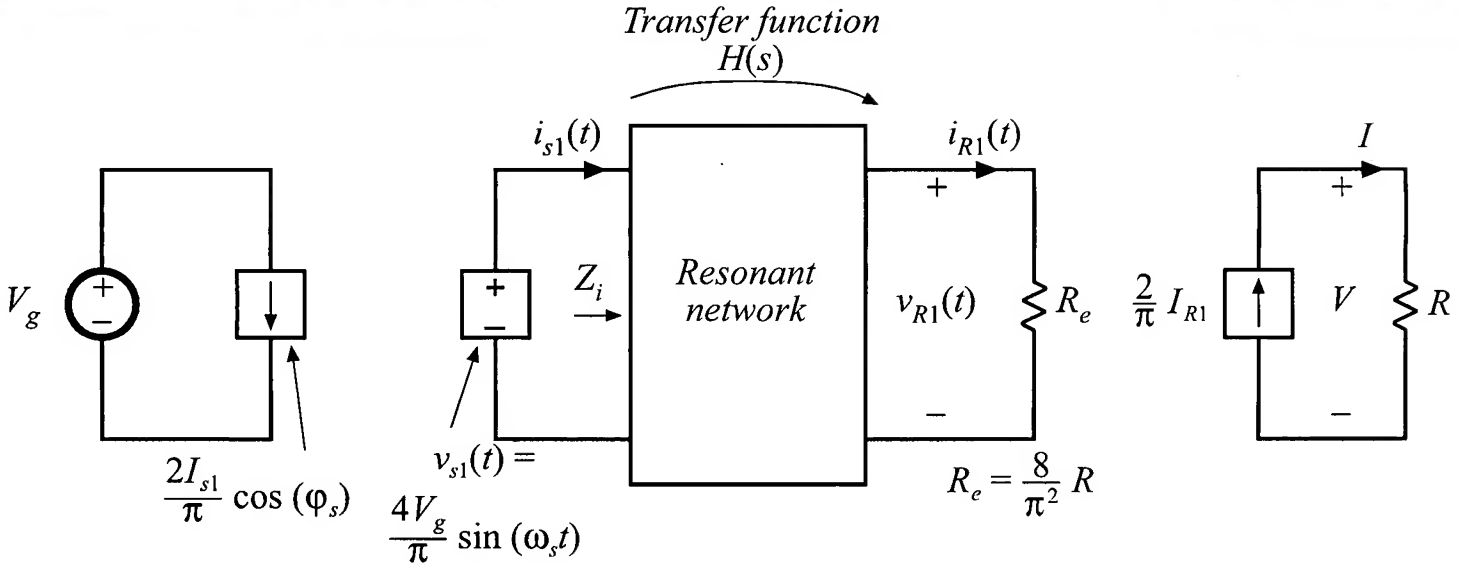
$$i_R(s) = \frac{v_{R1}(s)}{R_e} = \frac{H(s)}{R_e} v_{s1}(s)$$

which has peak magnitude

$$I_{R1} = \frac{\left\| H(s) \right\|_{s = j\omega_s}}{R_e} V_{s1}$$



19.1.4 Solution of converter voltage conversion ratio $M = V / V_g$



$$M = \frac{V}{V_g} = \underbrace{(R)}_{\left(\frac{V}{I}\right)} \underbrace{\left(\frac{2}{\pi}\right)}_{\left(\frac{I}{I_{R1}}\right)} \underbrace{\left(\frac{1}{R_e}\right)}_{\left(\frac{I_{R1}}{V_{R1}}\right)} \underbrace{\left(\| H(s) \|_{s=j\omega_s}\right)}_{\left(\frac{V_{R1}}{V_{s1}}\right)} \underbrace{\left(\frac{4}{\pi}\right)}_{\left(\frac{V_{s1}}{V_g}\right)}$$

Eliminate R_e:

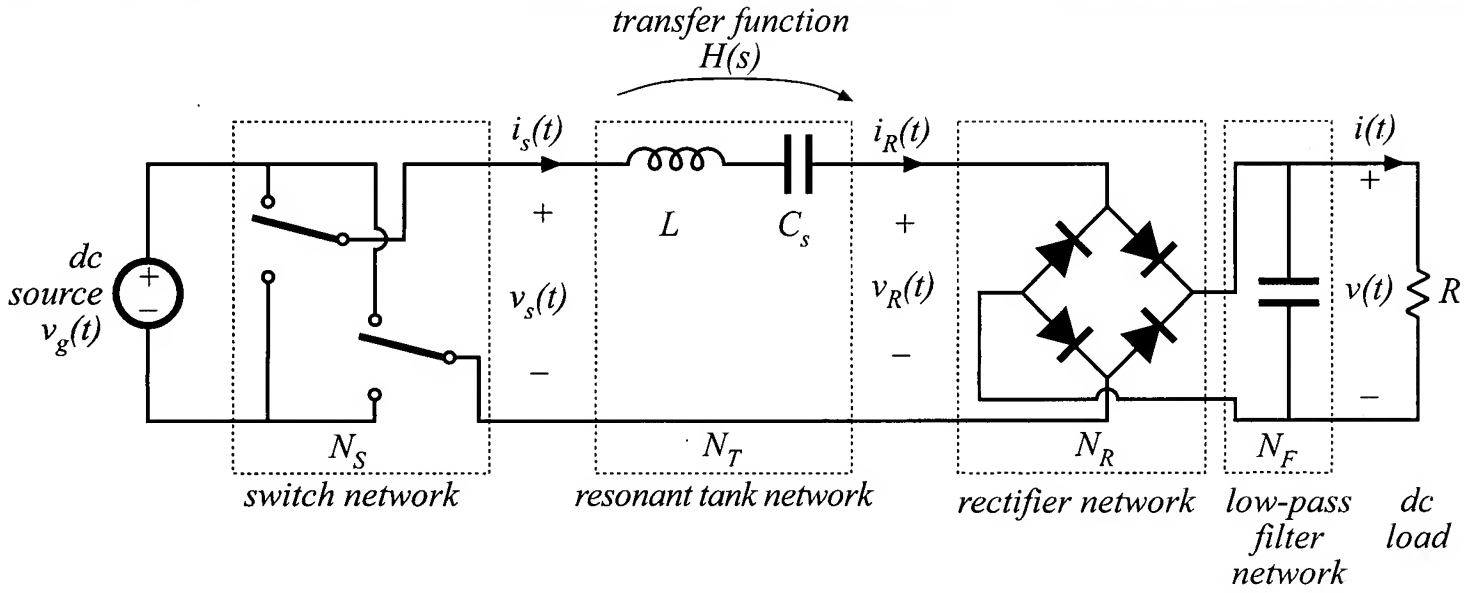
$$\frac{V}{V_g} = \| H(s) \|_{s=j\omega_s}$$

Conversion ratio M

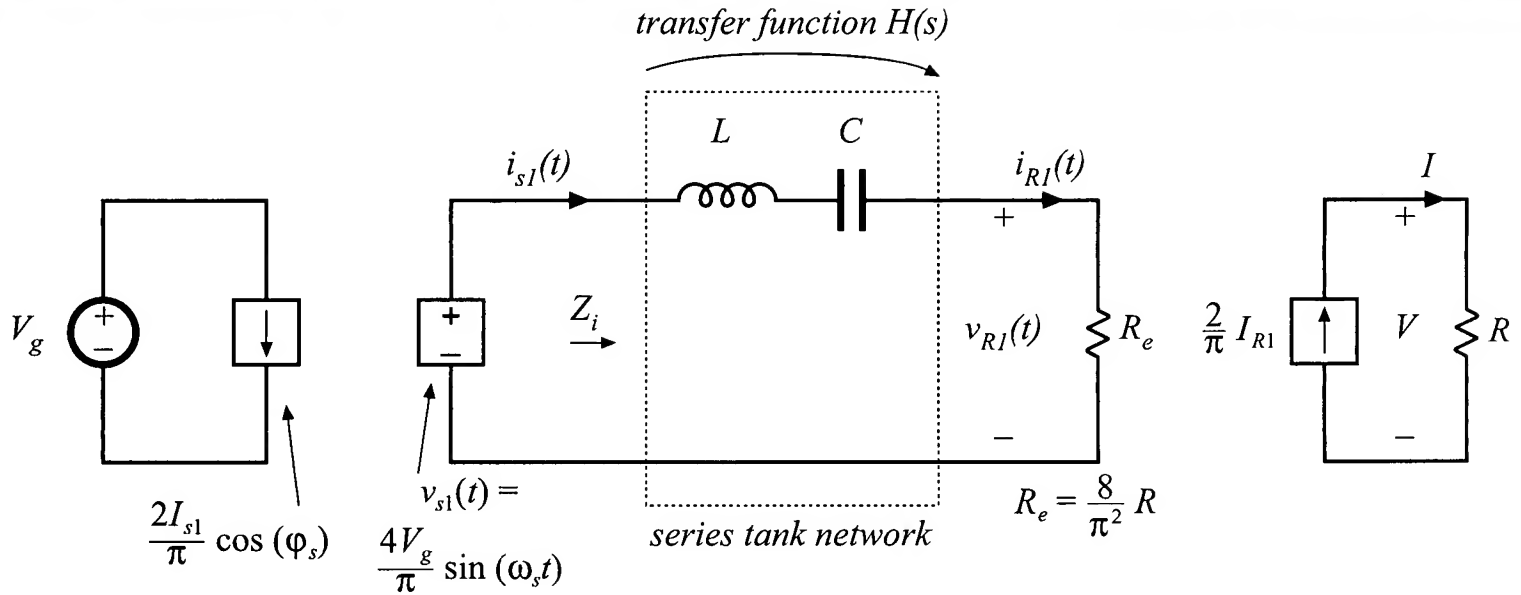
$$\frac{V}{V_g} = \left\| H(s) \right\|_{s = j\omega_s}$$

So we have shown that the conversion ratio of a resonant converter, having switch and rectifier networks as in previous slides, is equal to the magnitude of the tank network transfer function. This transfer function is evaluated with the tank loaded by the effective rectifier input resistance R_e.

19.2 Examples
19.2.1 Series resonant converter



Model: series resonant converter



$$H(s) = \frac{R_e}{Z_i(s)} = \frac{R_e}{R_e + sL + \frac{1}{sC}}$$

$$= \frac{\left(\frac{s}{Q_e \omega_0}\right)}{1 + \left(\frac{s}{Q_e \omega_0}\right) + \left(\frac{s}{\omega_0}\right)^2}$$

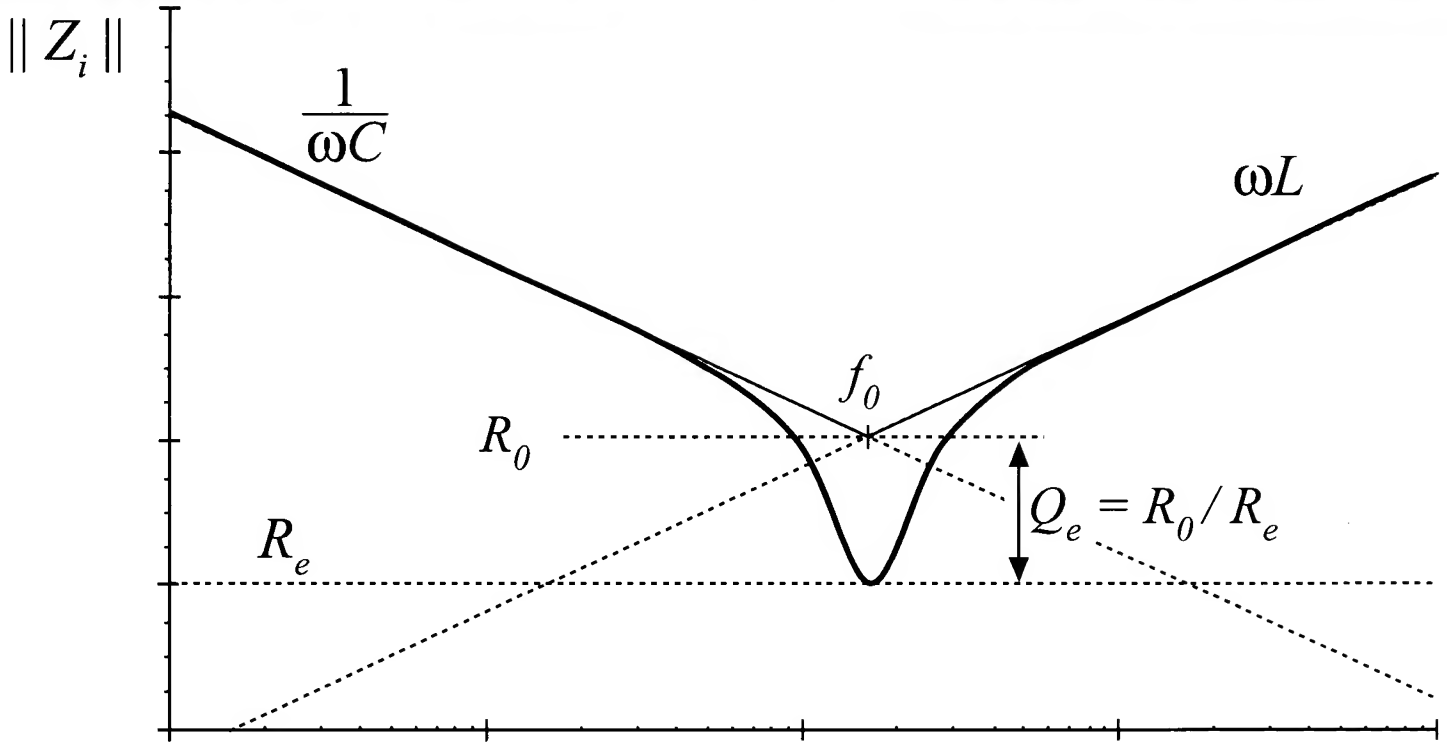
$$\omega_0 = \frac{1}{\sqrt{LC}} = 2\pi f_0$$

$$R_0 = \sqrt{\frac{L}{C}}$$

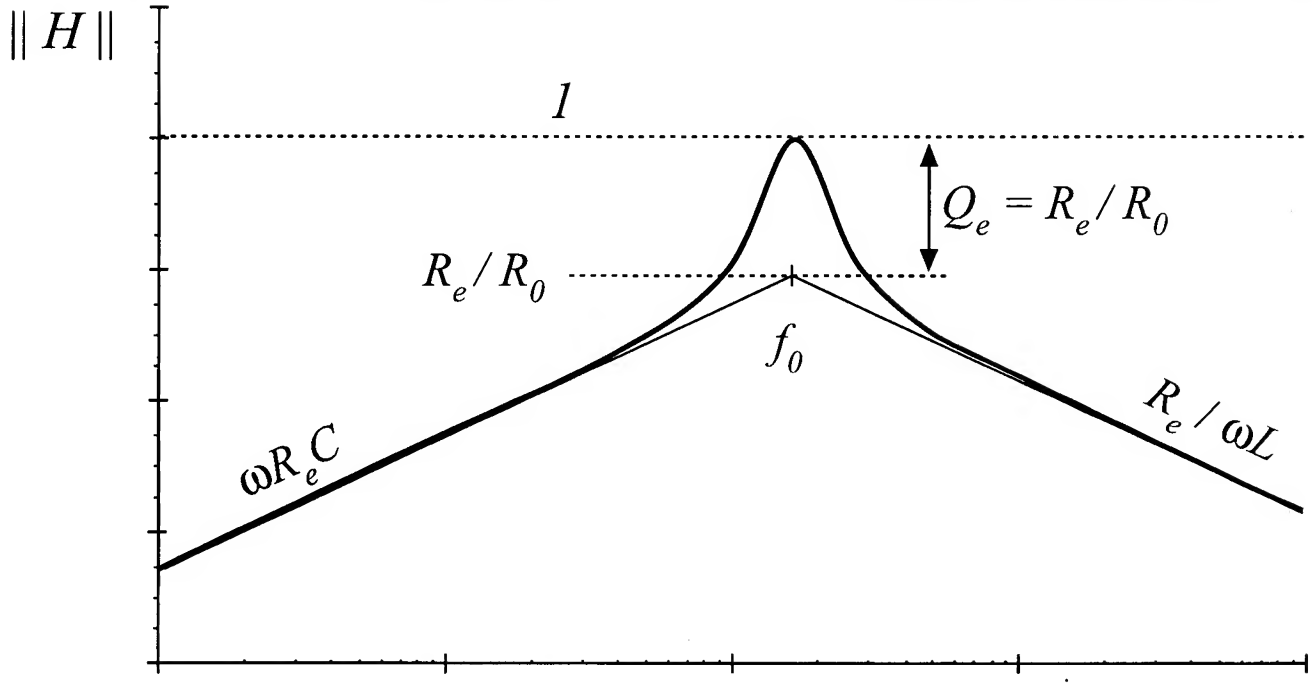
$$Q_e = \frac{R_0}{R_e}$$

$$M = \| H(j\omega_s) \| = \frac{1}{\sqrt{1 + Q_e^2 \left(\frac{1}{F} - F\right)^2}}$$

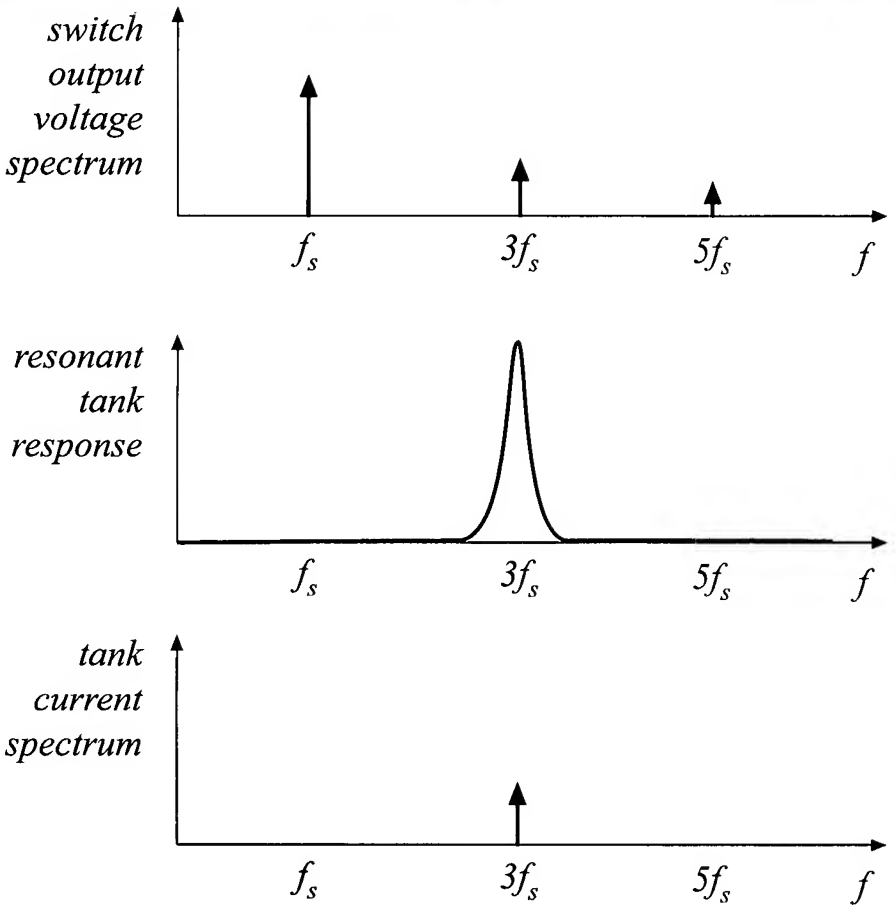
Construction of Z_i



Construction of H



19.2.2 Subharmonic modes of the SRC



Example: excitation of tank by third harmonic of switching frequency

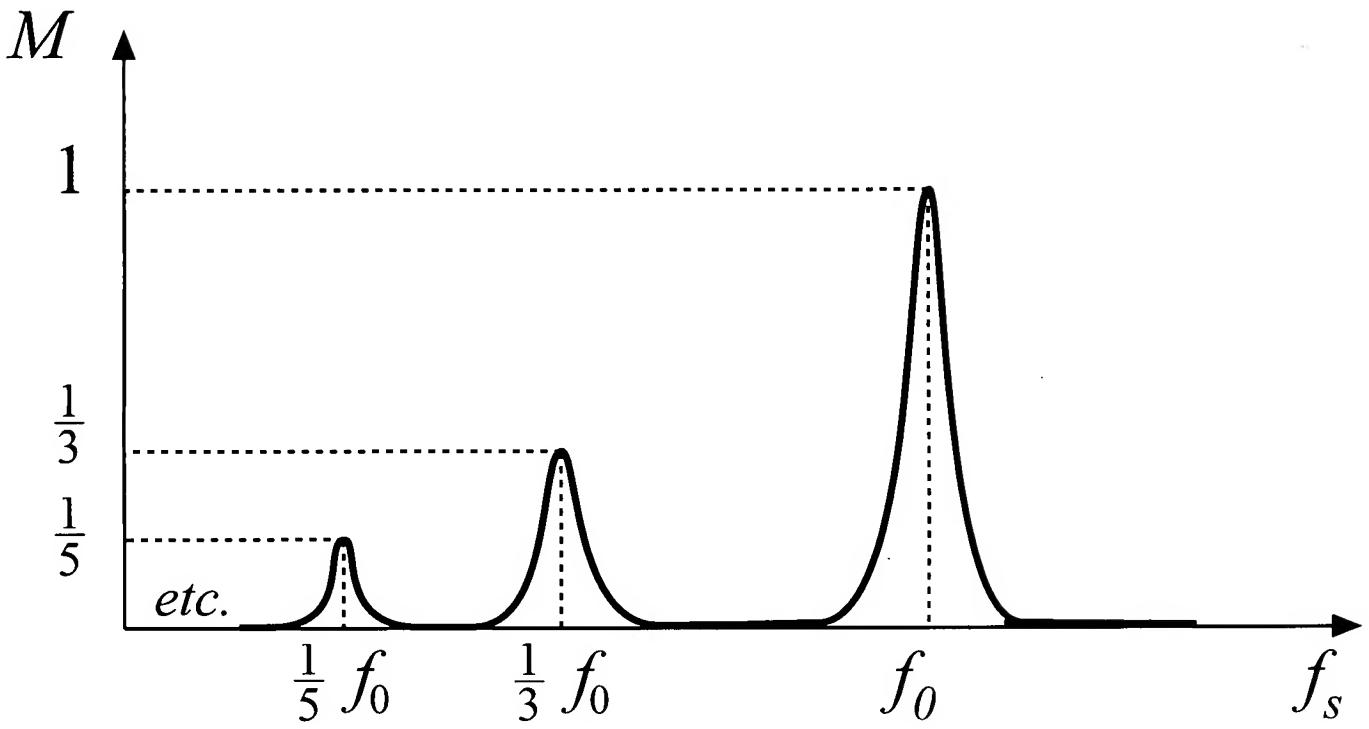
Can now approximate $v_s(t)$ by its third harmonic:

$$v_s(t) \approx v_{sn}(t) = \frac{4V_g}{n\pi} \sin(n\omega_s t)$$

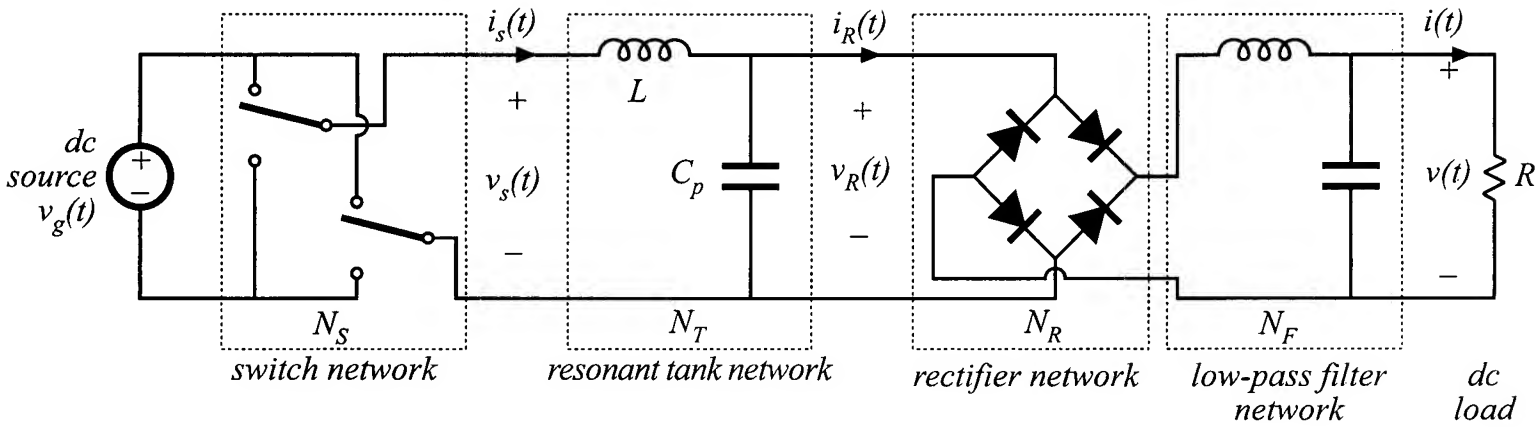
Result of analysis:

$$M = \frac{V}{V_g} = \frac{\| H(jn\omega_s) \|}{n}$$

Subharmonic modes of SRC



19.2.3 Parallel resonant dc-dc converter



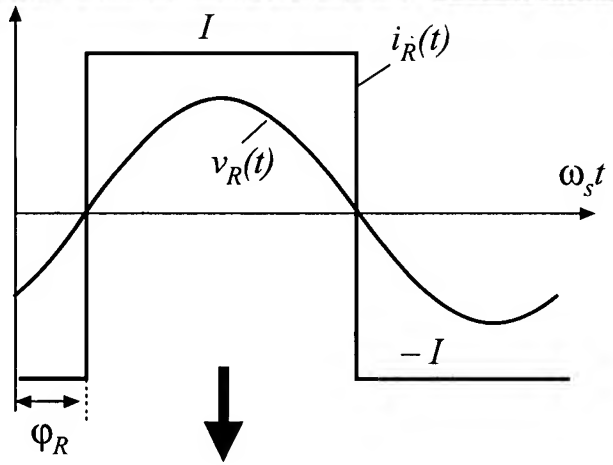
Differs from series resonant converter as follows:

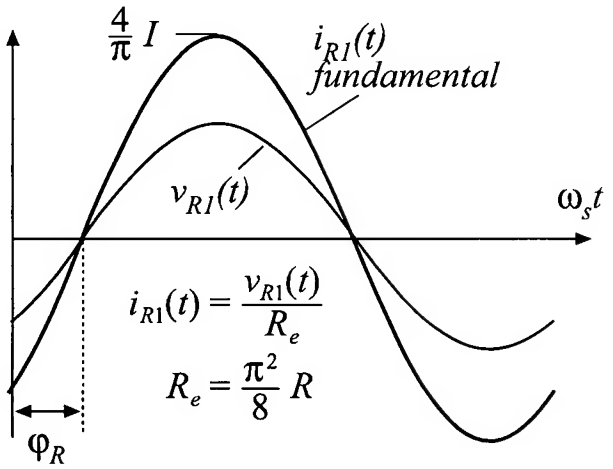
Different tank network

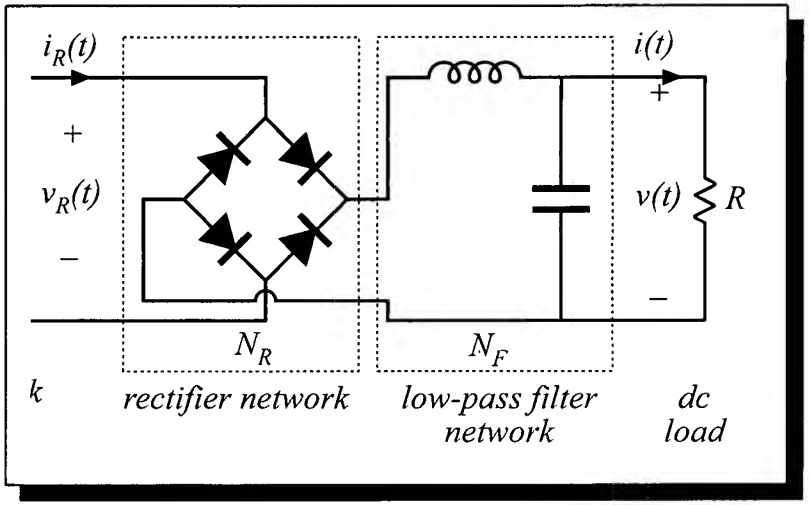
Rectifier is driven by sinusoidal voltage, and is connected to inductive-input low-pass filter

Need a new model for rectifier and filter networks

Model of uncontrolled rectifier with inductive filter network







Fundamental component of $i_R(t)$:

$$i_{R1}(t) = \frac{4I}{\pi} \sin(\omega_s t - \varphi_R)$$

Effective resistance R_e

Again define

$$R_e = \frac{v_{R1}(t)}{i_{R1}(t)} = \frac{\pi V_{R1}}{4I}$$

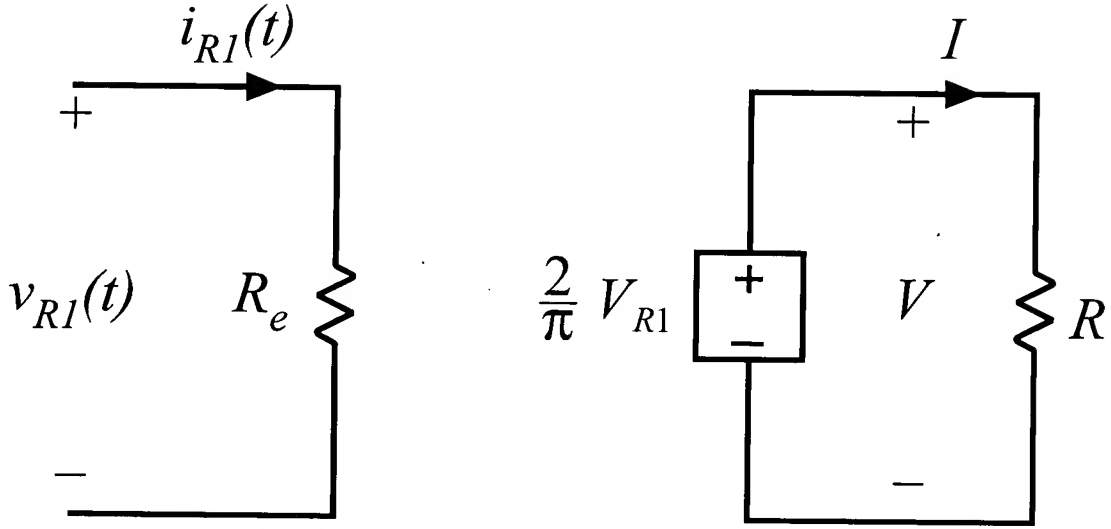
In steady state, the dc output voltage V is equal to the average value of $|\, v_R \,|$:

$$V = \frac{2}{T_S} \int_0^{T_S/2} V_{R1} \left| \sin(\omega_s t - \varphi_R) \right| dt = \frac{2}{\pi} V_{R1}$$

For a resistive load, $V = IR$. The effective resistance R_e can then be expressed

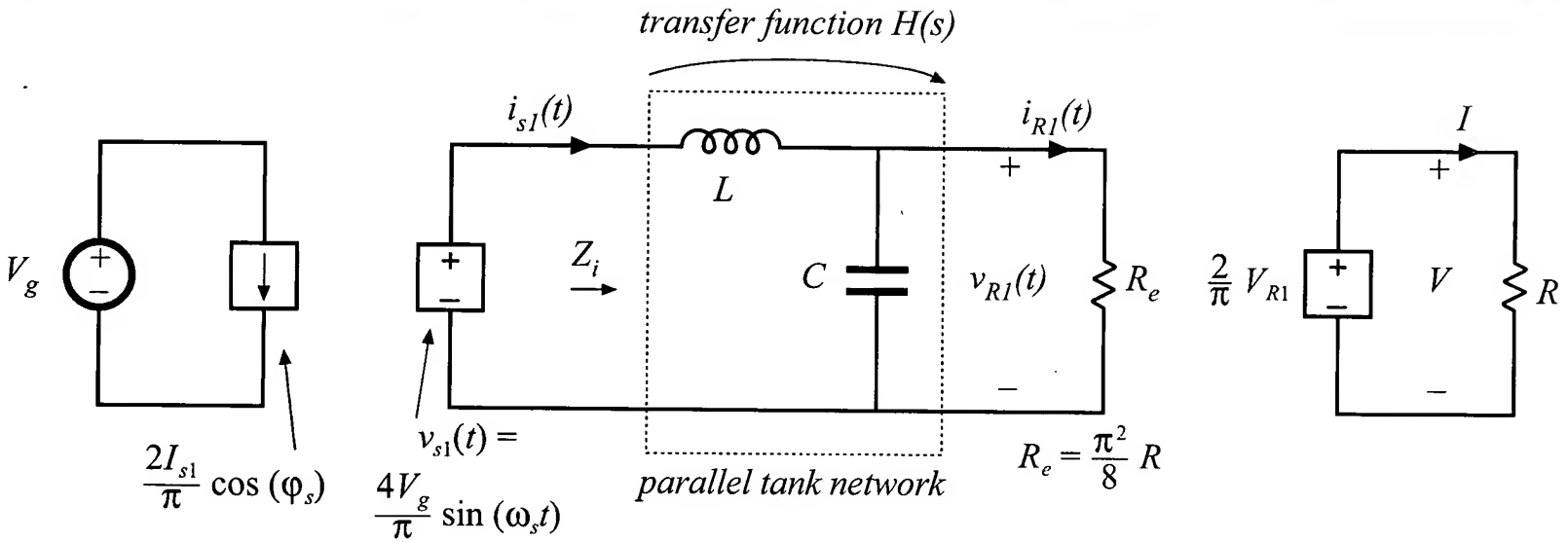
$$R_e = \frac{\pi^2}{8} R = 1.2337R$$

Equivalent circuit model of uncontrolled rectifier with inductive filter network



$$R_e = \frac{\pi^2}{8} R$$

Equivalent circuit model
Parallel resonant dc-dc converter

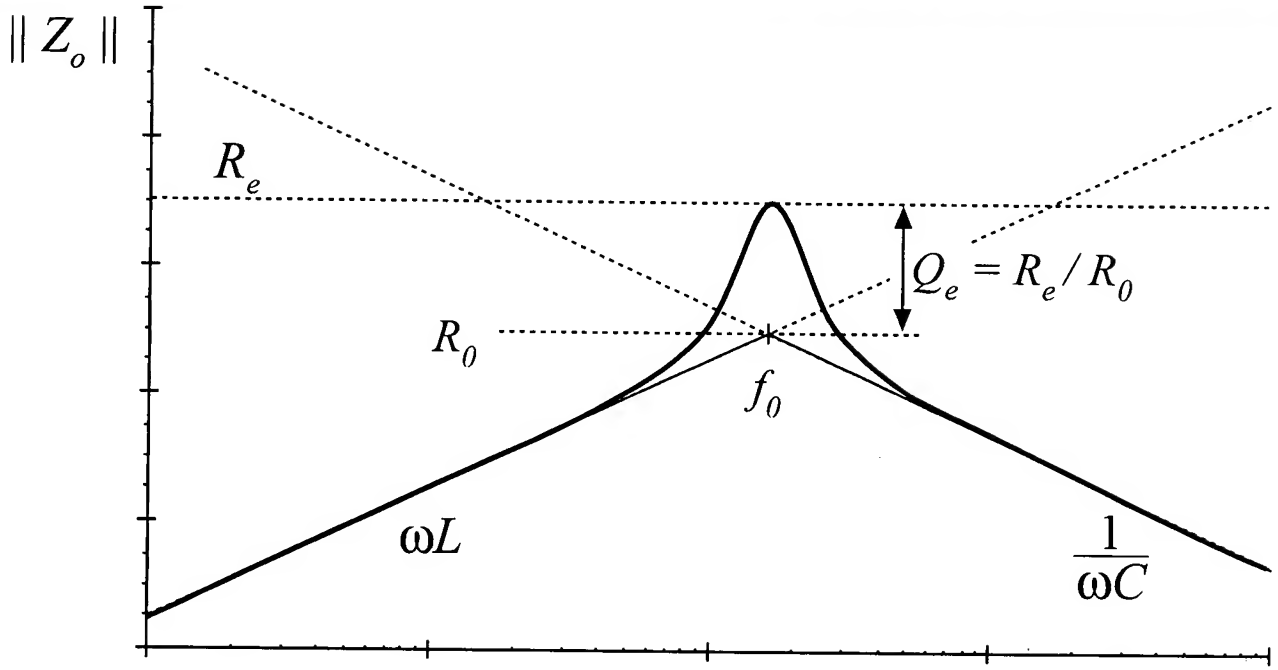


$$M = \frac{V}{V_g} = \frac{8}{\pi^2} \left\| H(s) \right\|_{s = j\omega_s}$$

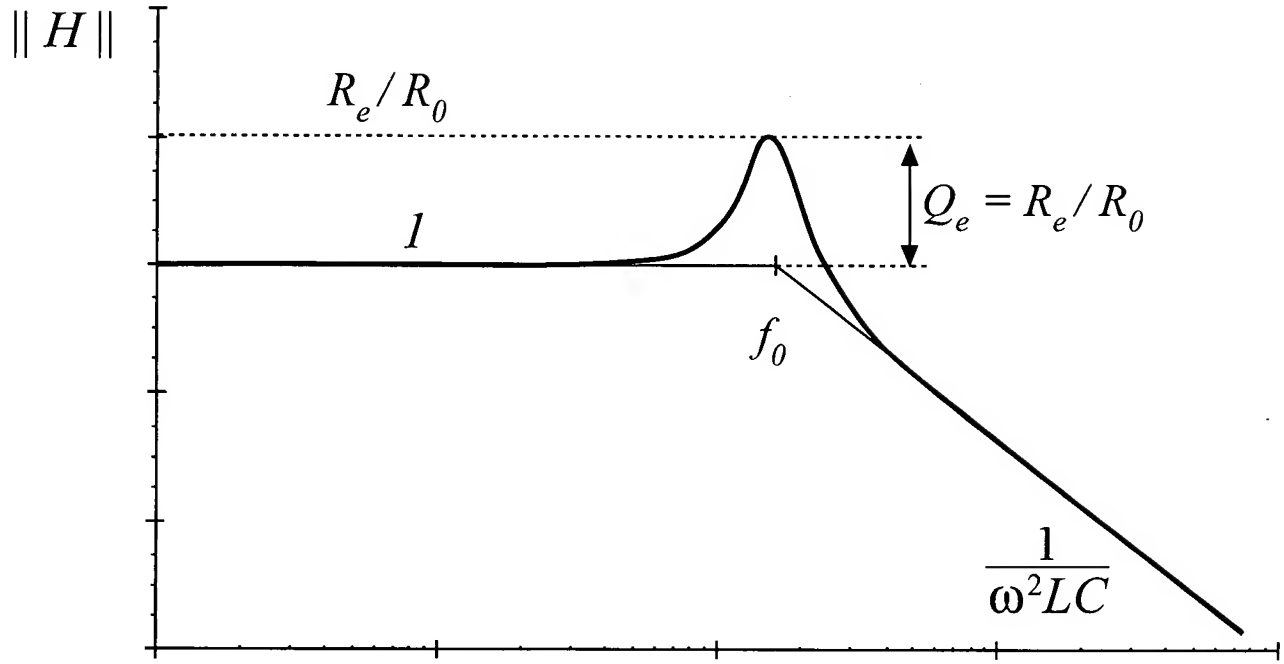
$$H(s) = \frac{Z_o(s)}{sL}$$

$$Z_o(s) = sL \,||\, \frac{1}{sC} \,||\, R_e$$

Construction of Z_o



Construction of H



Dc conversion ratio of the PRC

$$M = \frac{8}{\pi^2} \left\| \frac{Z_o(s)}{sL} \right\|_{s = j\omega_s} = \frac{8}{\pi^2} \left\| \frac{1}{1 + \frac{s}{Q_e \omega_0} + \left(\frac{s}{\omega_0} \right)^2} \right\|_{s = j\omega_s}$$

$$= \frac{8}{\pi^2} \frac{1}{\sqrt{\left(1 - F^2\right)^2 + \left(\frac{F}{Q_e} \right)^2}}$$

At resonance, this becomes $M = \frac{8}{\pi^2} \frac{R_e}{R_0} = \frac{R}{R_0}$

- PRC can step up the voltage, provided $R > R_0$
- PRC can produce M approaching infinity, provided output current is limited to value less than V_g / R_0

19.3 Exact characteristics of the series and parallel resonant dc-dc converters

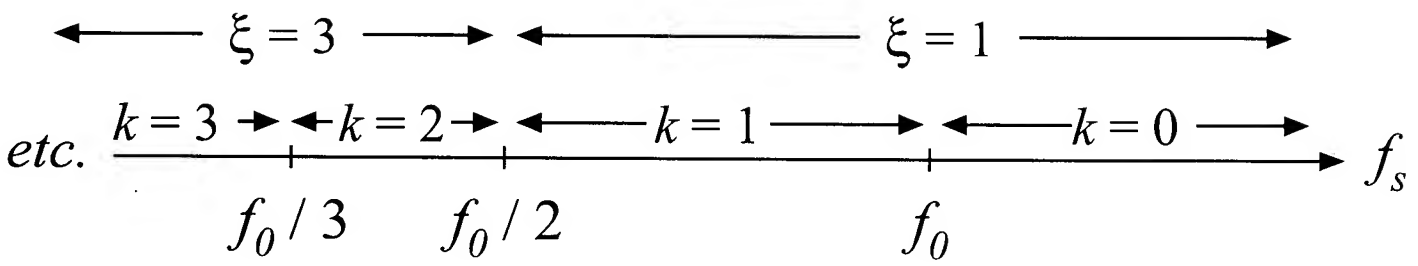
Define

$$\frac{f_0}{k+1} < f_s < \frac{f_0}{k} \quad \text{or} \quad \frac{1}{k+1} < F < \frac{1}{k}$$

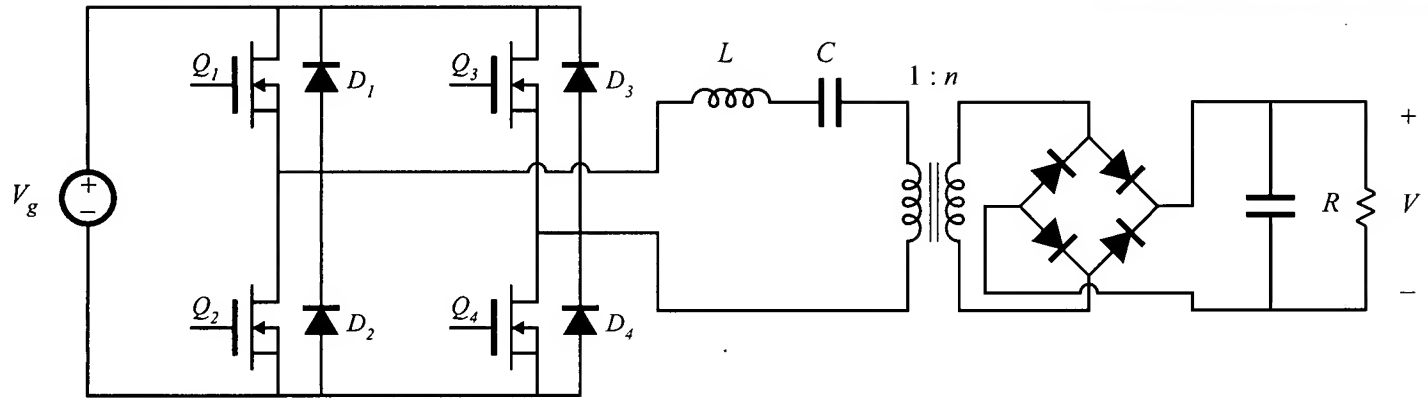
mode index k

$$\xi = k + \frac{1 + (-1)^k}{2}$$

subharmonic index ξ



19.3.1 Exact characteristics of the series resonant converter



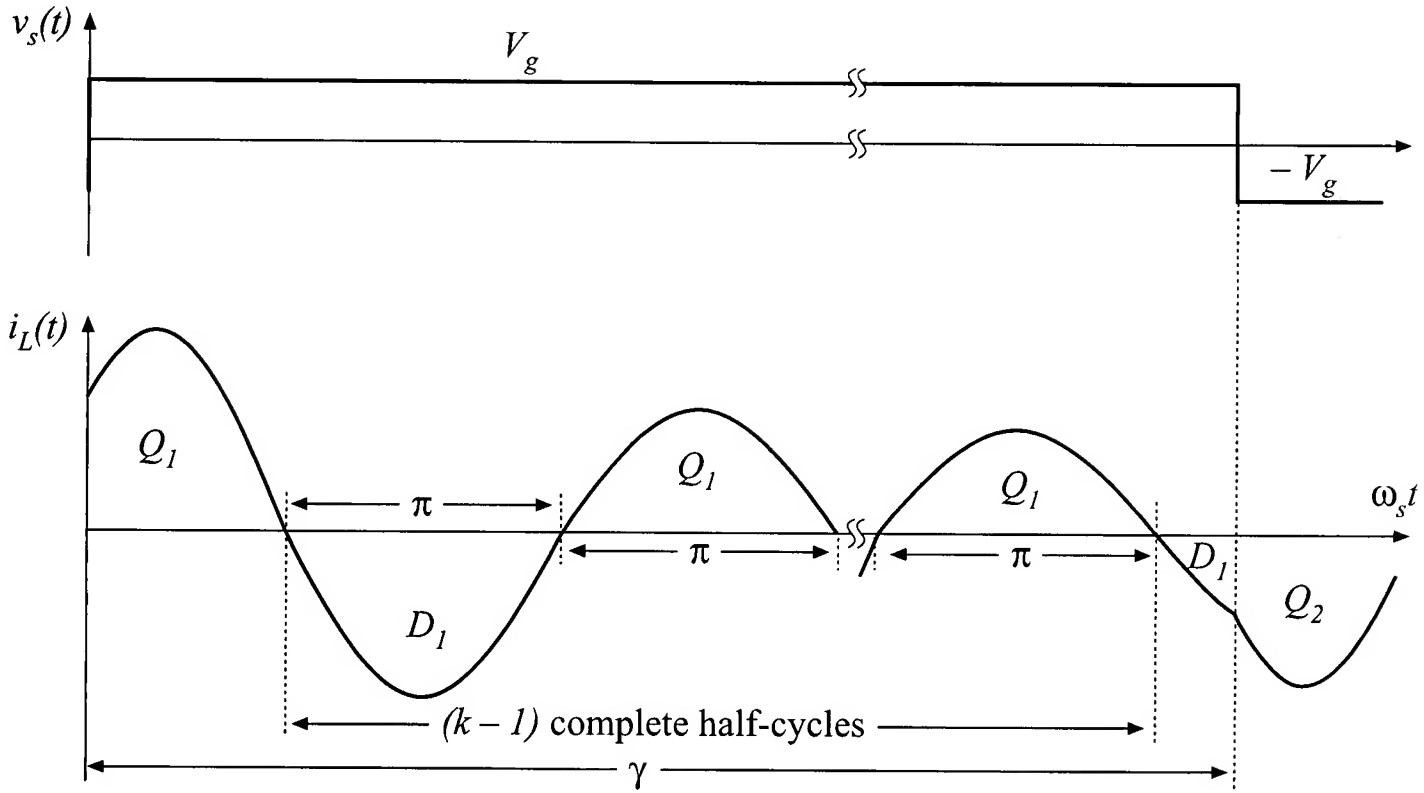
Normalized load voltage and current:

$$M = \frac{V}{nV_g} \qquad J = \frac{InR_0}{V_g}$$

Continuous conduction mode, SRC

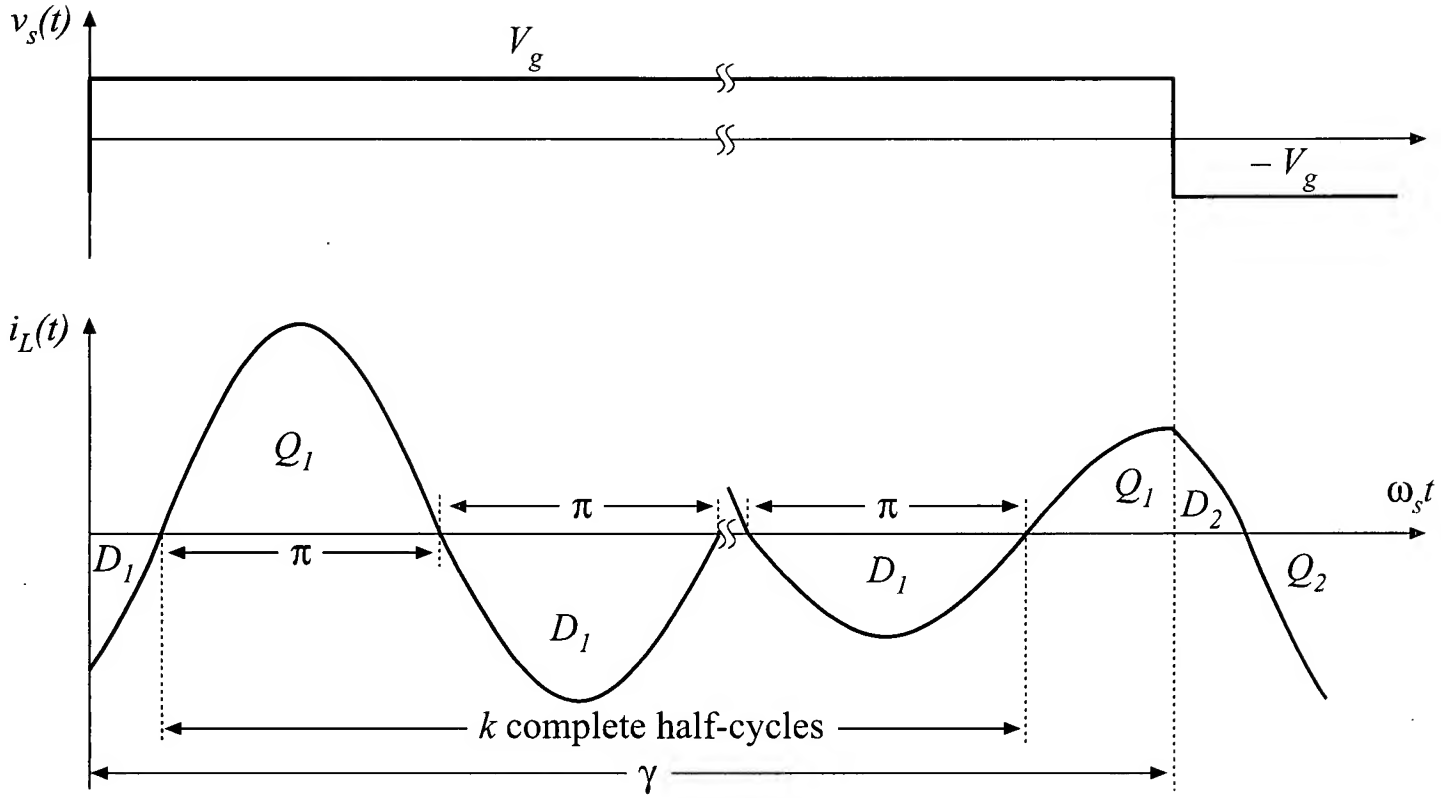
Tank current rings continuously for entire length of switching period

Waveforms for type k CCM, odd k :



Series resonant converter

Waveforms for type k CCM, even k :



Exact steady-state solution, CCM

Series resonant converter

$$M^2\xi^2 \sin^2\left(\frac{\gamma}{2}\right) + \frac{1}{\xi^2}\left(\frac{J\gamma}{2} + (-1)^k\right)^2 \cos^2\left(\frac{\gamma}{2}\right) = 1$$

where

$$M = \frac{V}{nV_g} \qquad J = \frac{InR_0}{V_g}$$

$$\gamma = \frac{\omega_0 T_s}{2} = \frac{\pi}{F}$$

- Output characteristic, i.e., the relation between M and J, is elliptical
- M is restricted to the range

$$0 \le M \le \frac{1}{\xi}$$

Control-plane characteristics

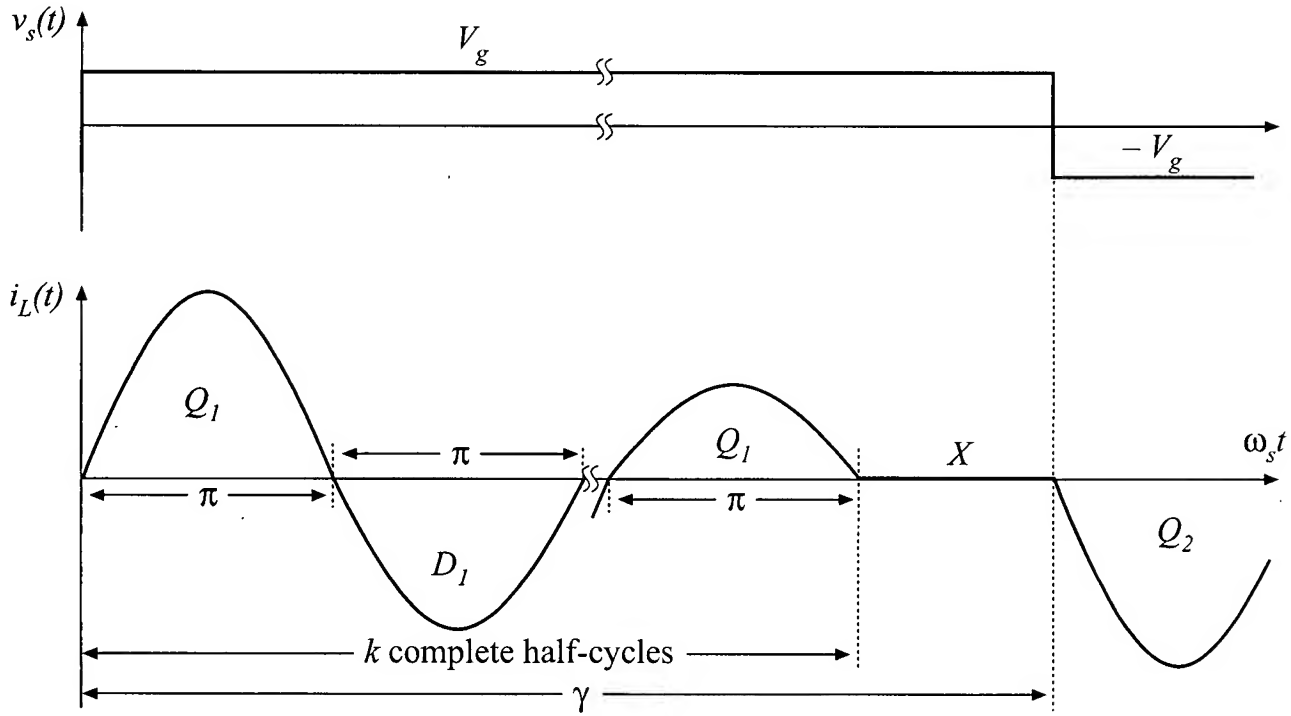
For a resistive load, eliminate J and solve for M vs. γ

$$M = \frac{\left(\frac{Q\gamma}{2}\right)}{\xi^4 \tan^2\left(\frac{\gamma}{2}\right) + \left(\frac{Q\gamma}{2}\right)^2} \left[(-1)^{k+1} + \sqrt{1 + \frac{\left[\xi^2 - \cos^2\left(\frac{\gamma}{2}\right)\right]\left[\xi^4 \tan^2\left(\frac{\gamma}{2}\right) + \left(\frac{Q\gamma}{2}\right)^2\right]}{\left(\frac{Q\gamma}{2}\right)^2 \cos^2\left(\frac{\gamma}{2}\right)}} \right]$$

Exact, closed-form, valid for any CCM

Discontinuous conduction mode

Type k DCM: during each half-switching-period, the tank rings for k complete half-cycles. The output diodes then become reverse-biased for the remainder of the half-switching-period.



Steady-state solution: type k DCM, odd k

$$M = \frac{1}{k}$$

Conditions for operation in type k DCM, odd k :

$$f_s < \frac{f_0}{k}$$

$$\frac{2(k+1)}{\gamma} > J > \frac{2(k-1)}{\gamma}$$

Steady-state solution: type k DCM, even k

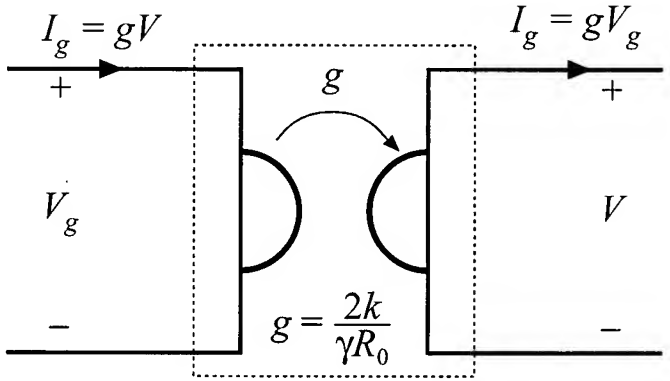
$$J = \frac{2k}{\gamma}$$

Conditions for operation in type k DCM, even k :

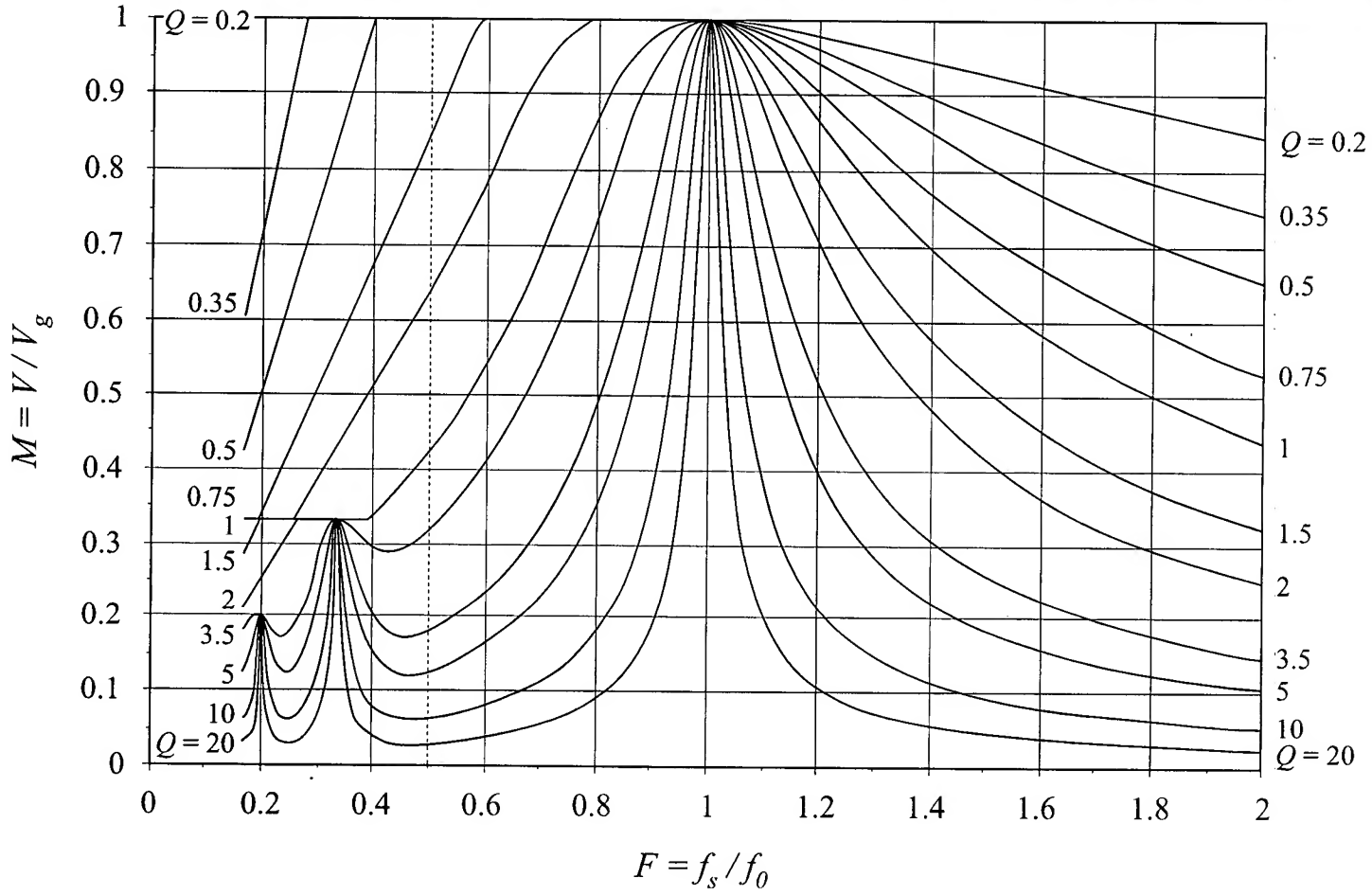
$$f_s < \frac{f_0}{k}$$

$$\frac{1}{k-1} > M > \frac{1}{k+1}$$

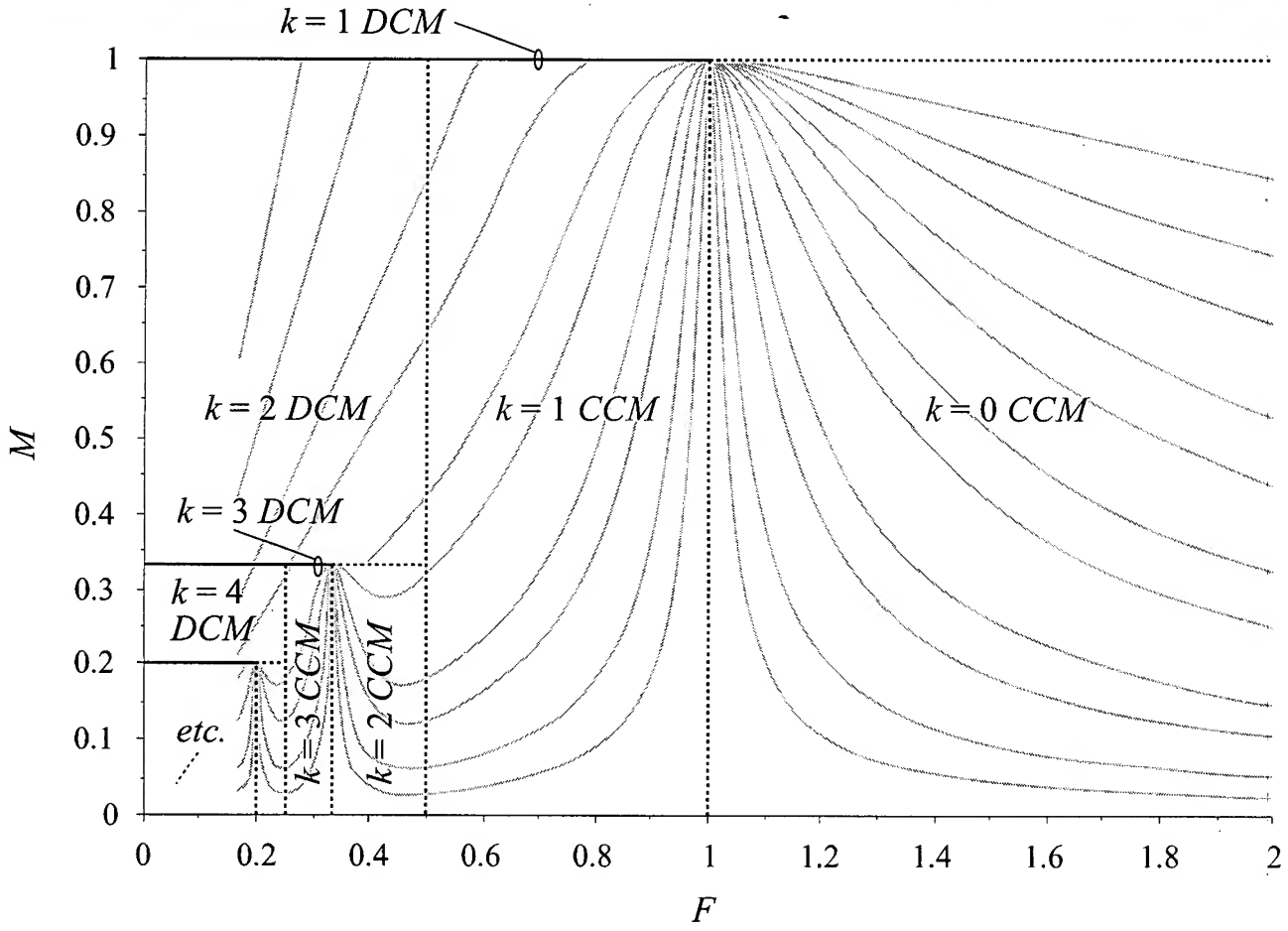
gyrator model, SRC operating in an even DCM:



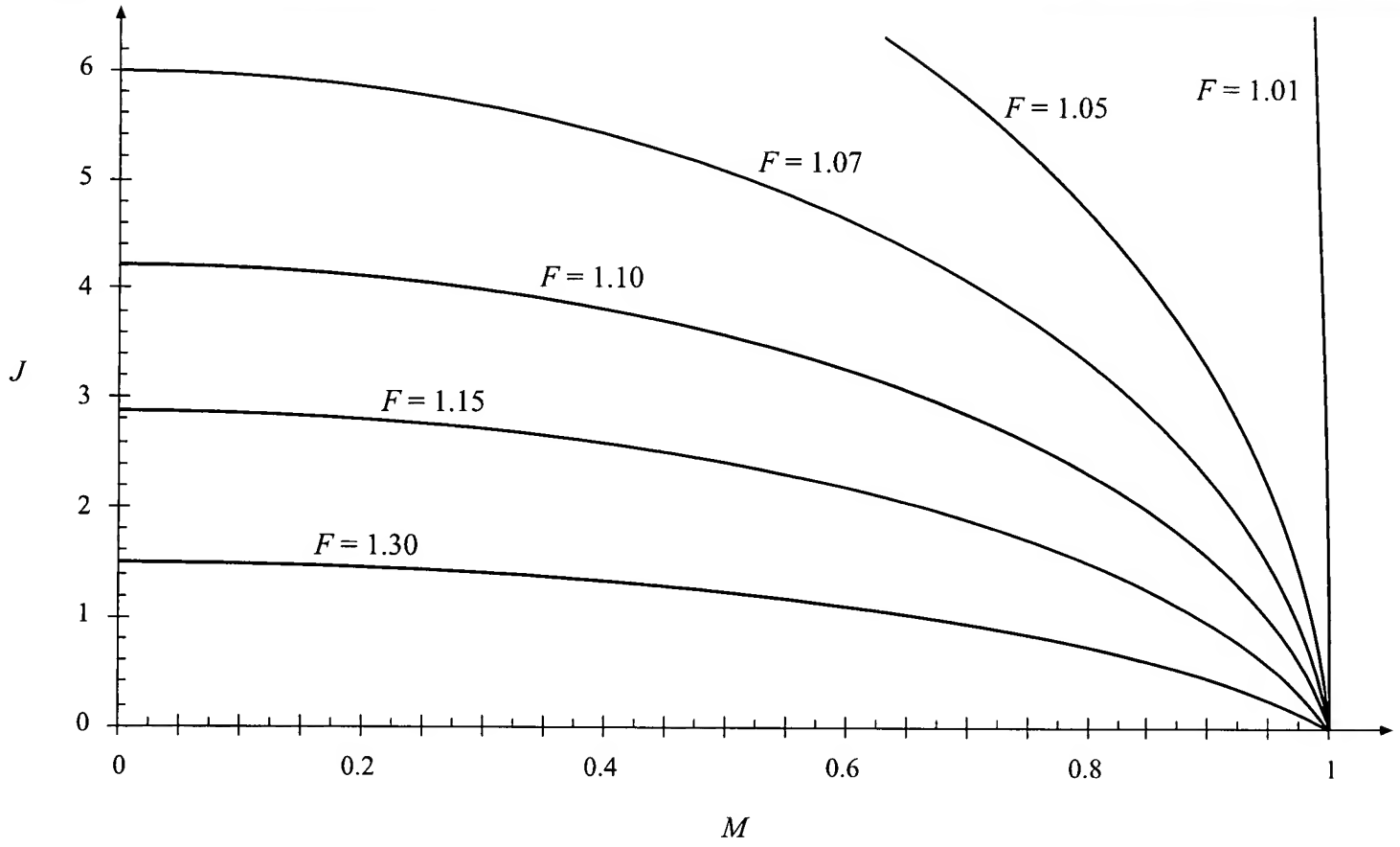
Control plane characteristics, SRC



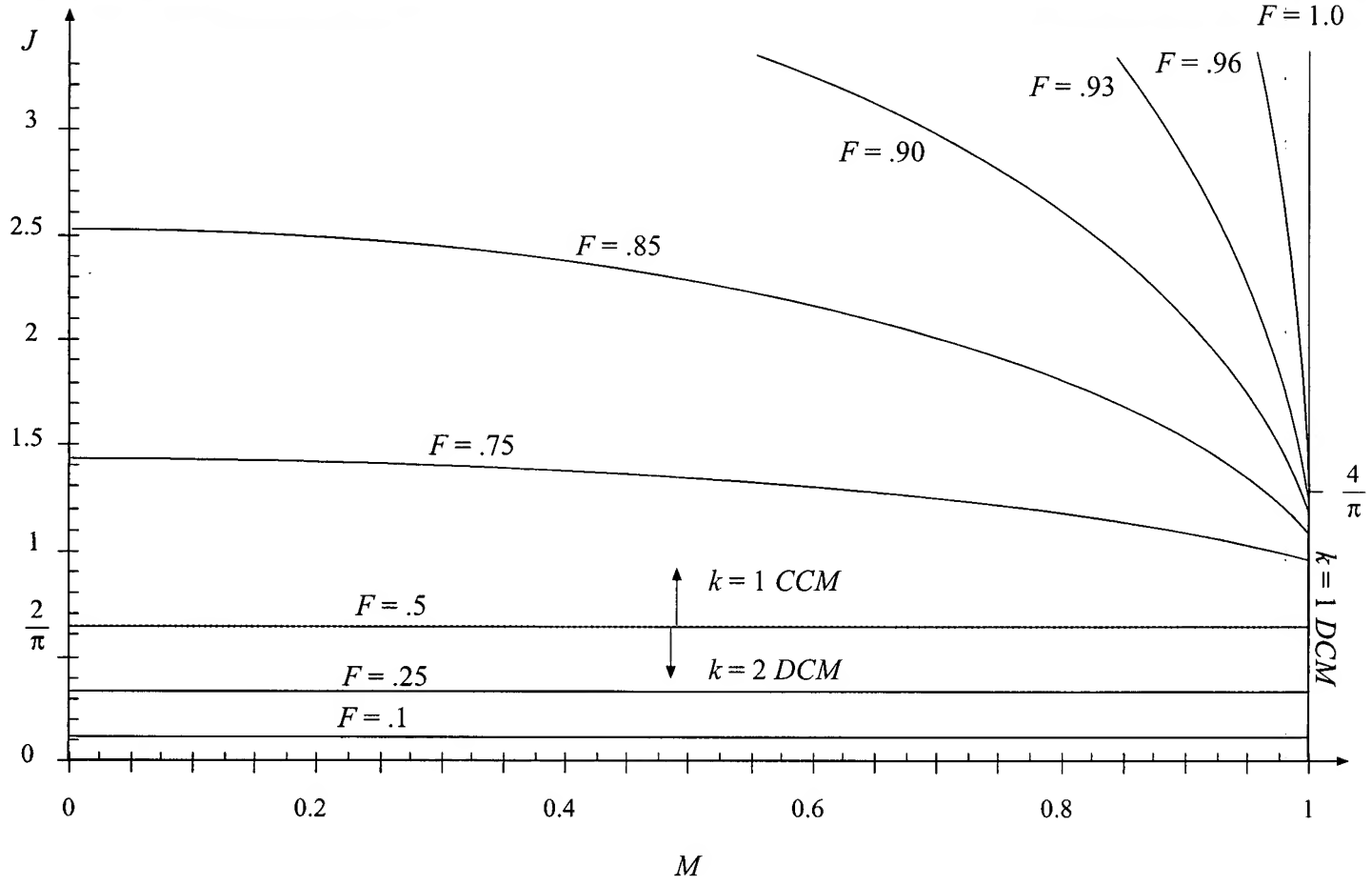
Mode boundaries, SRC



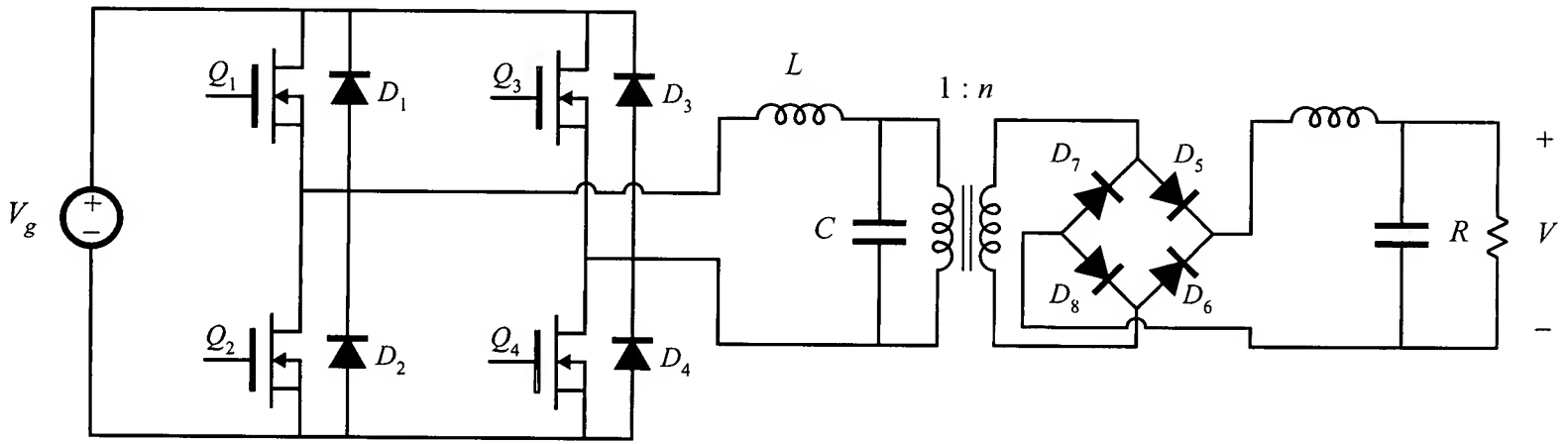
Output characteristics, SRC above resonance



Output characteristics, SRC below resonance



19.3.2 Exact characteristics of the parallel resonant converter



Normalized load voltage and current:

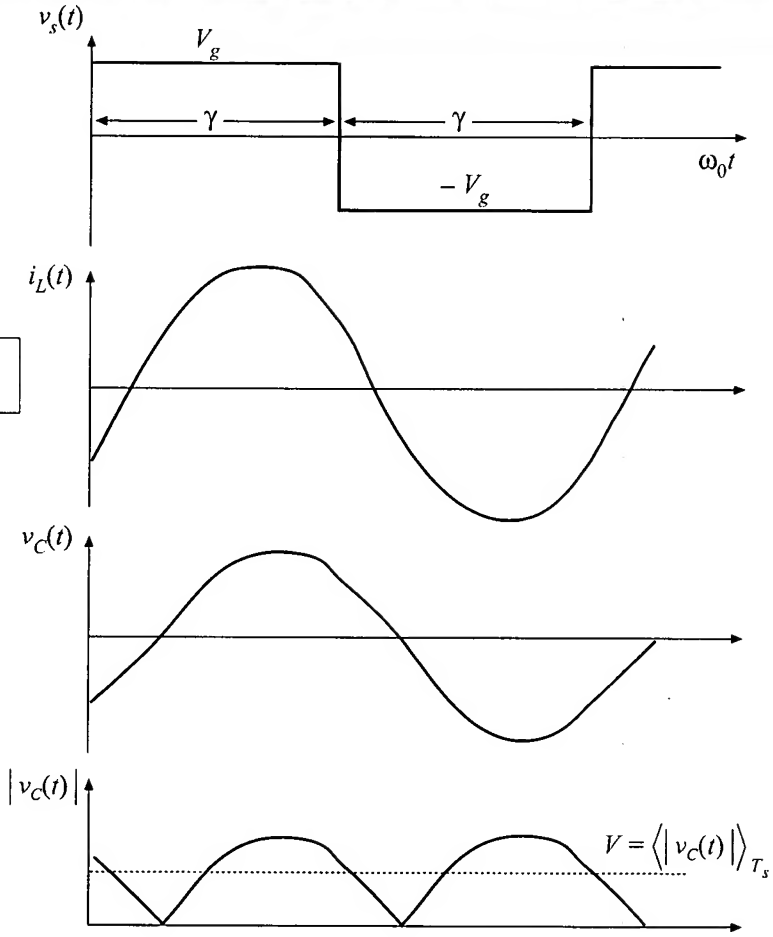
$$M = \frac{V}{nV_g} \qquad J = \frac{InR_0}{V_g}$$

Parallel resonant converter in CCM

CCM closed-form solution

$$M = \left(\frac{2}{\gamma}\right)\left(\varphi - \frac{\sin(\varphi)}{\cos\left(\frac{\gamma}{2}\right)}\right)$$

$$\varphi = \begin{cases} -\cos^{-1}\left(\cos\left(\frac{\gamma}{2}\right) + J\sin\left(\frac{\gamma}{2}\right)\right) & \text{for } 0 < \gamma < \pi \\ +\cos^{-1}\left(\cos\left(\frac{\gamma}{2}\right) + J\sin\left(\frac{\gamma}{2}\right)\right) & \text{for } \pi < \gamma < 2\pi \end{cases}$$



Parallel resonant converter in DCM

Mode boundary

$J > J_{crit}(\gamma)$ for DCM

$J < J_{crit}(\gamma)$ for CCM

$$J_{crit}(\gamma) = -\frac{1}{2}\sin(\gamma) + \sqrt{\sin^2\left(\frac{\gamma}{2}\right) + \frac{1}{4}\sin^2(\gamma)}$$

DCM equations

$$M_{C0} = 1 - \cos(\beta)$$

$$J_{L0} = J + \sin(\beta)$$

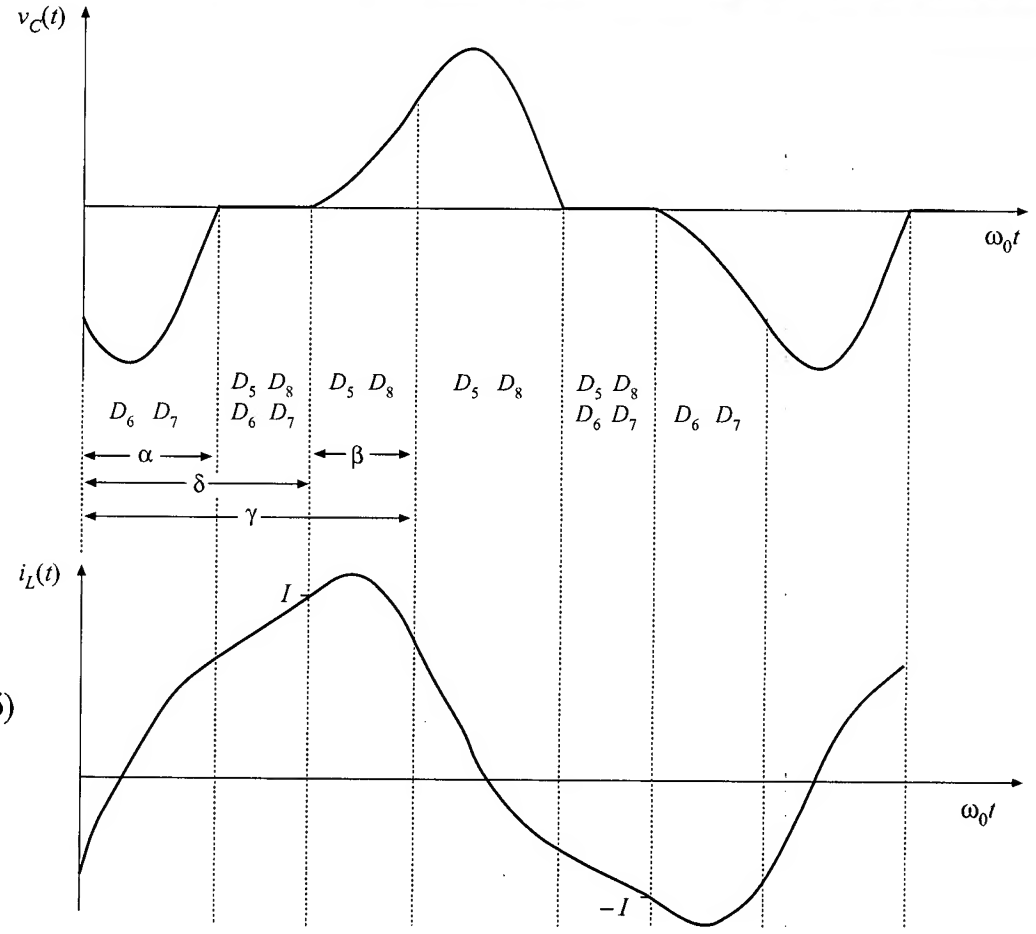
$$\cos(\alpha+\beta) - 2\cos(\alpha) = -1$$

$$-\sin(\alpha+\beta) + 2\sin(\alpha) + (\delta - \alpha) = 2J$$

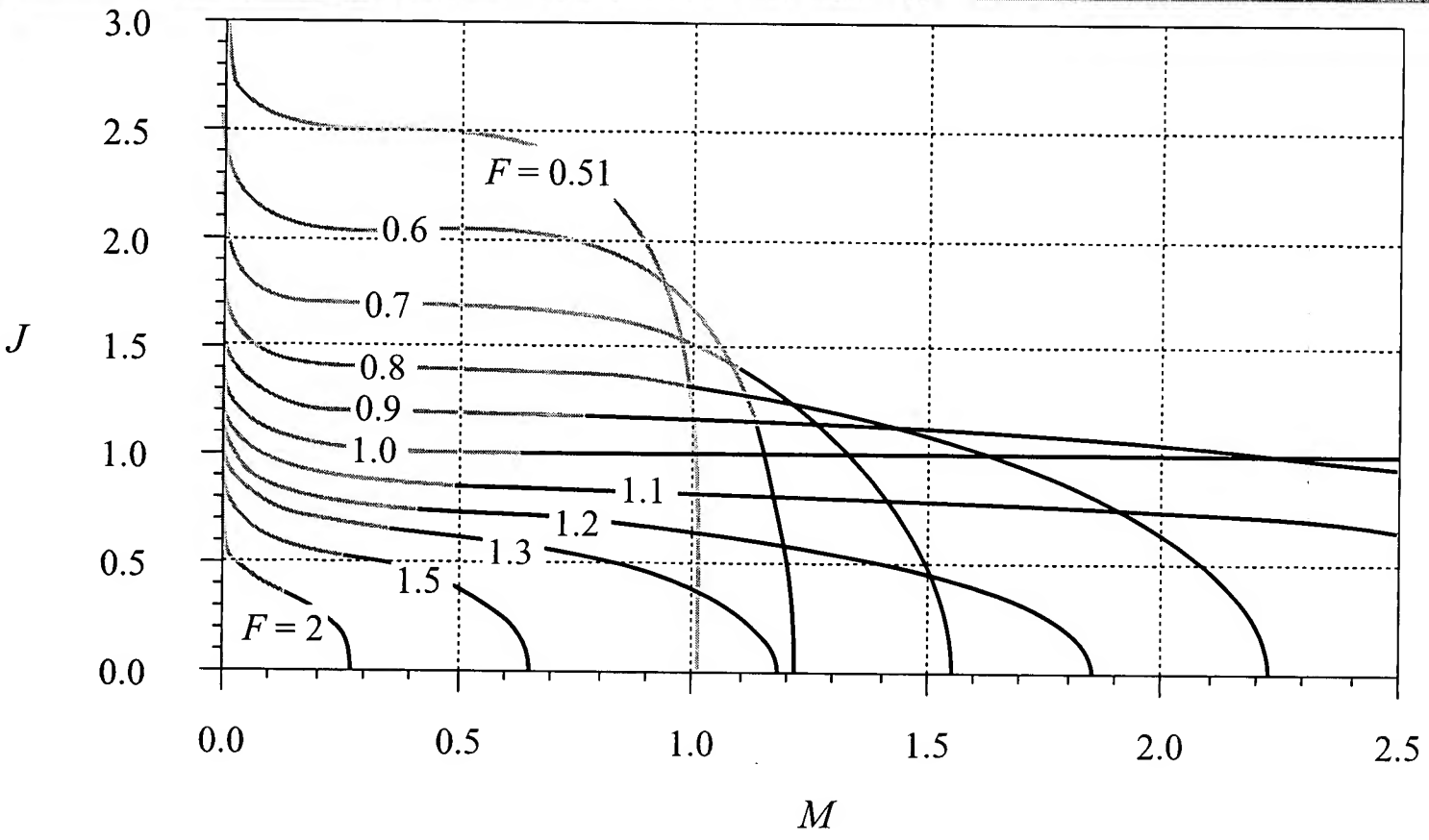
$$\beta + \delta = \gamma$$

$$M = 1 + \left(\frac{2}{\gamma}\right)(J - \delta)$$

(require iteration)



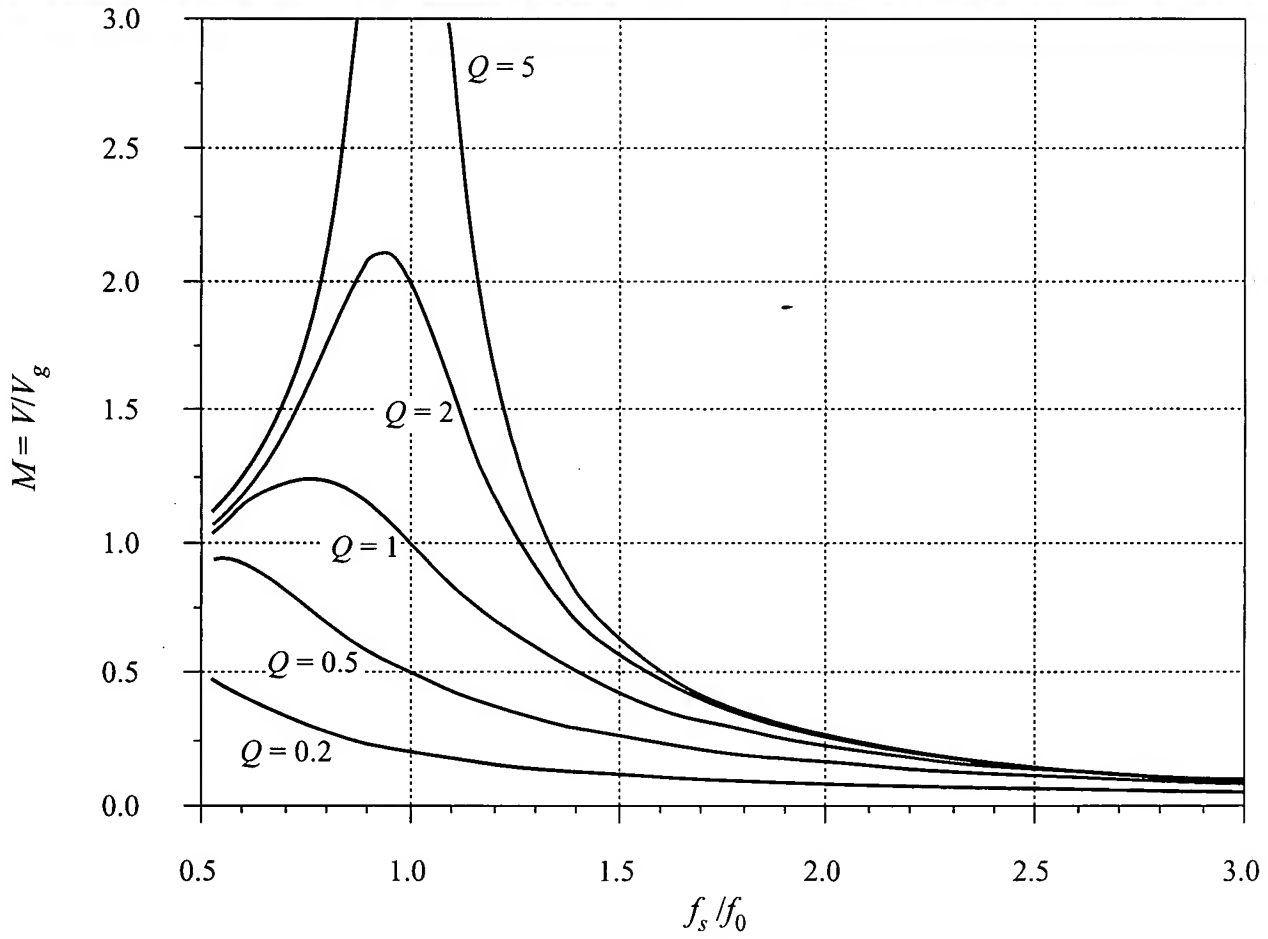
Output characteristics of the PRC



Solid curves: CCM Shaded curves: DCM

Control characteristics of the PRC

with resistive load



19.4 Soft switching

Soft switching can mitigate some of the mechanisms of switching loss and possibly reduce the generation of EMI

Semiconductor devices are switched on or off at the zero crossing of their voltage or current waveforms:

Zero-current switching: transistor turn-off transition occurs at zero current. Zero-current switching eliminates the switching loss caused by IGBT current tailing and by stray inductances. It can also be used to commutate SCR's.

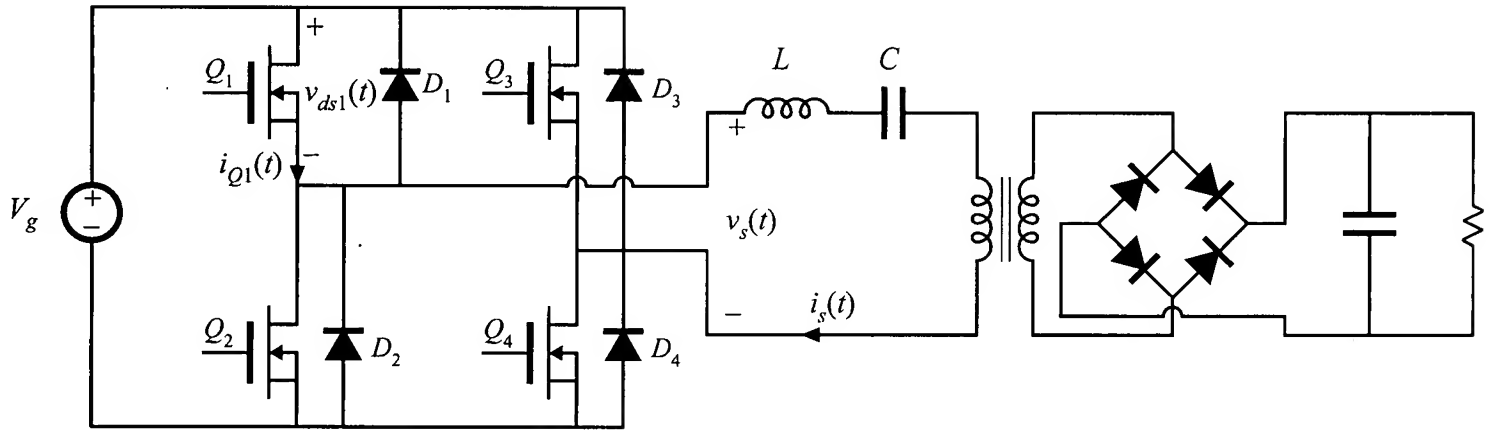
Zero-voltage switching: transistor turn-on transition occurs at zero voltage. Diodes may also operate with zero-voltage switching. Zero-voltage switching eliminates the switching loss induced by diode stored charge and device output capacitances.

Zero-voltage switching is usually preferred in modern converters.

Zero-voltage transition converters are modified PWM converters, in which an inductor charges and discharges the device capacitances. Zero-voltage switching is then obtained.

19.4.1 Operation of the full bridge below resonance: Zero-current switching

Series resonant converter example



Operation below resonance: input tank current leads voltage

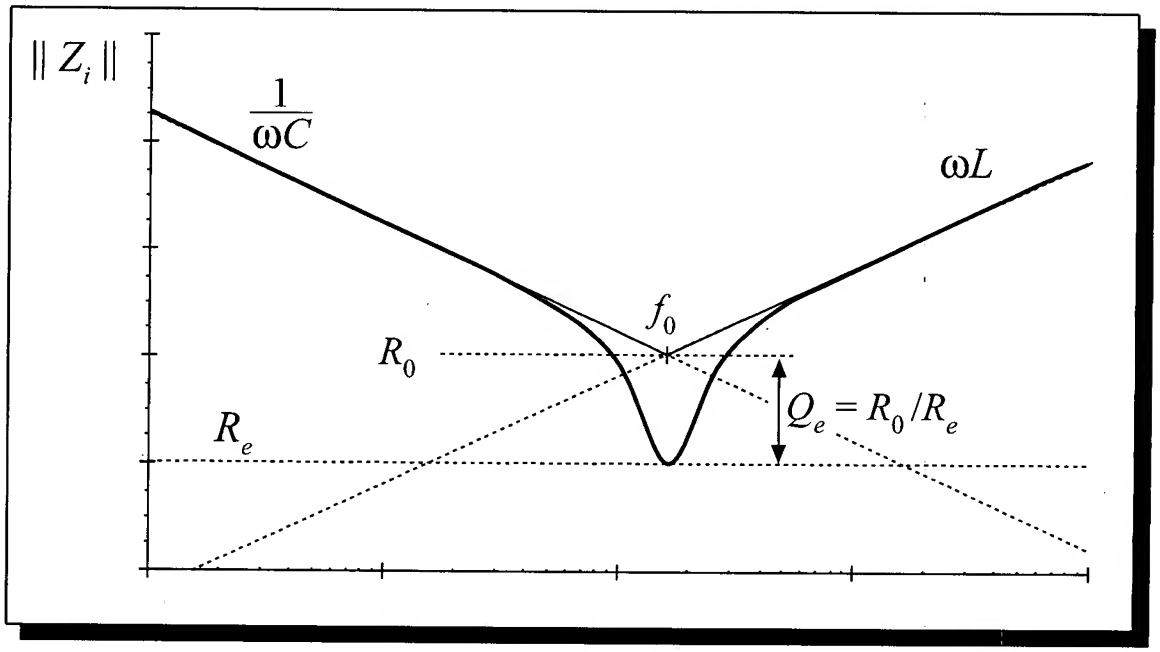
Zero-current switching (ZCS) occurs

Tank input impedance

Operation below resonance: tank input impedance Z_i is dominated by tank capacitor.

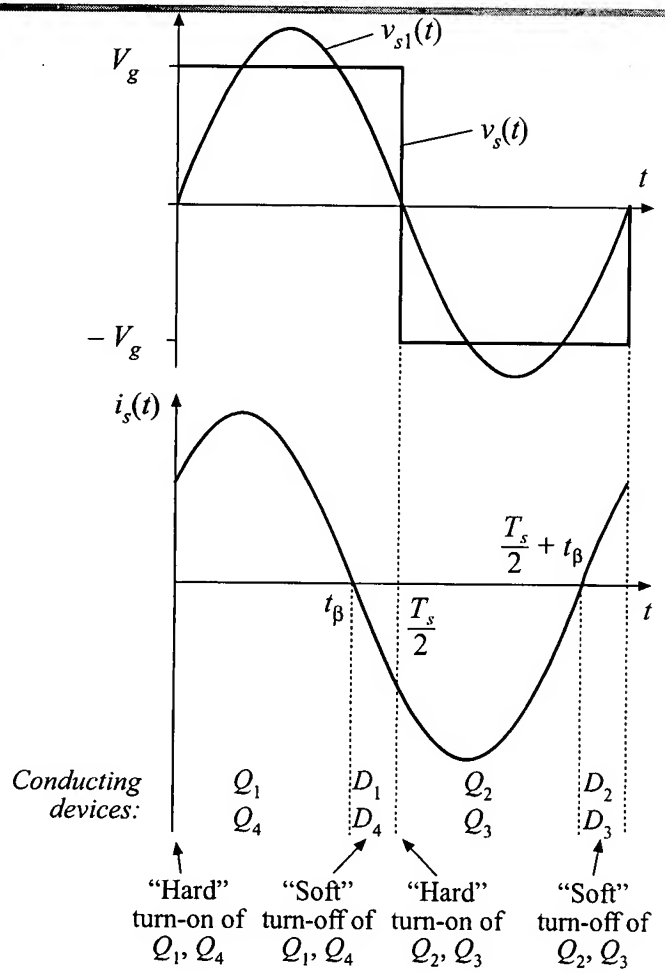
$\angle Z_i$ is positive, and tank input current leads tank input voltage.

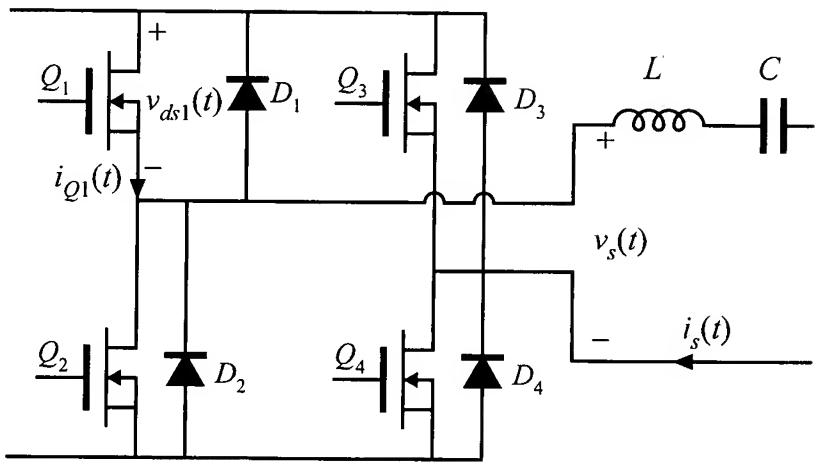
Zero crossing of the tank input current waveform $i_s(t)$ occurs before the zero crossing of the voltage $v_s(t)$.



Switch network waveforms, below resonance

Zero-current switching

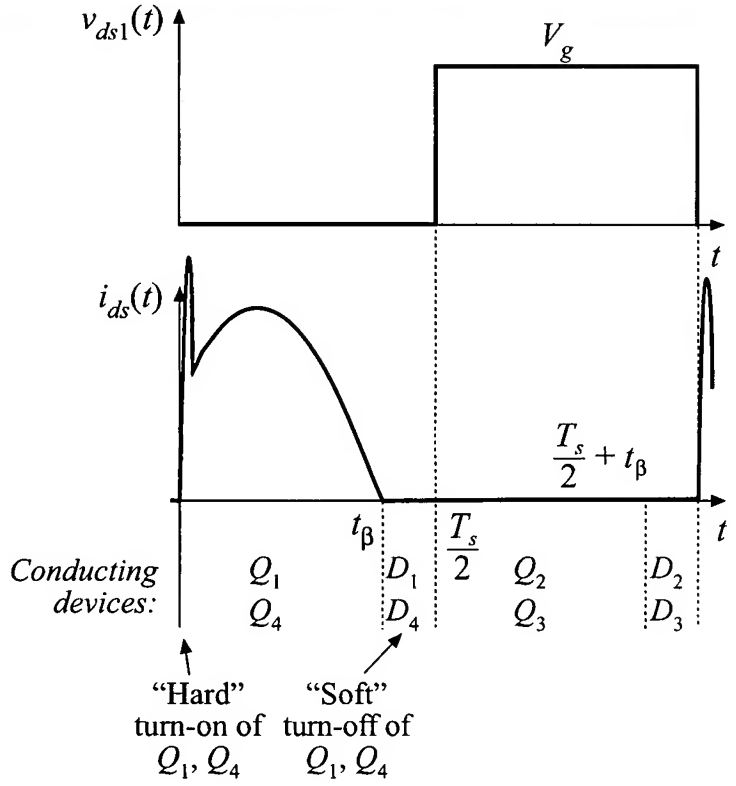


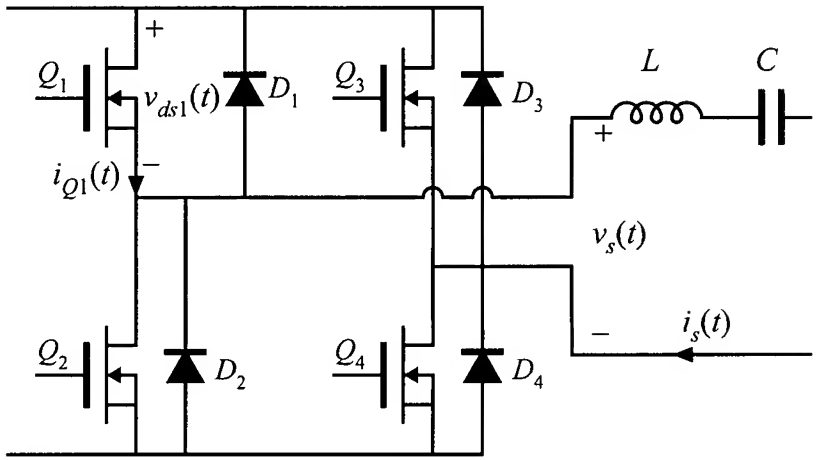


Conduction sequence: Q_1–D_1–Q_2–D_2

Q_1 is turned off during D_1 conduction interval, without loss

ZCS turn-on transition: hard switching

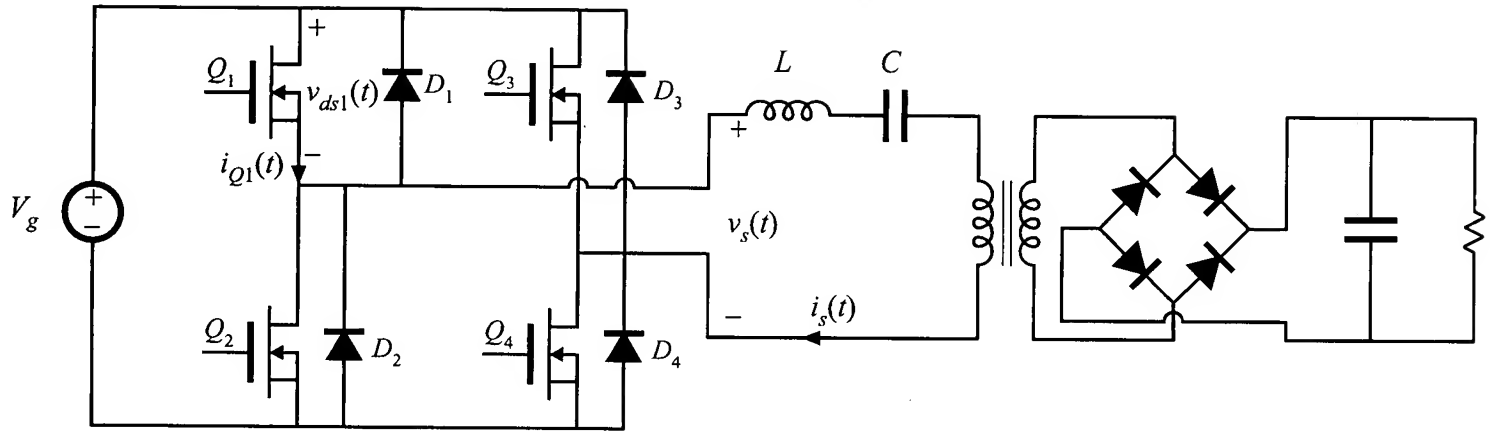




Q_1 turns on while D_2 is conducting. Stored charge of D_2 and of semiconductor output capacitances must be removed. Transistor turn-on transition is identical to hard-switched PWM, and switching loss occurs.

19.4.2 Operation of the full bridge below resonance: Zero-voltage switching

Series resonant converter example



Operation above resonance: input tank current lags voltage

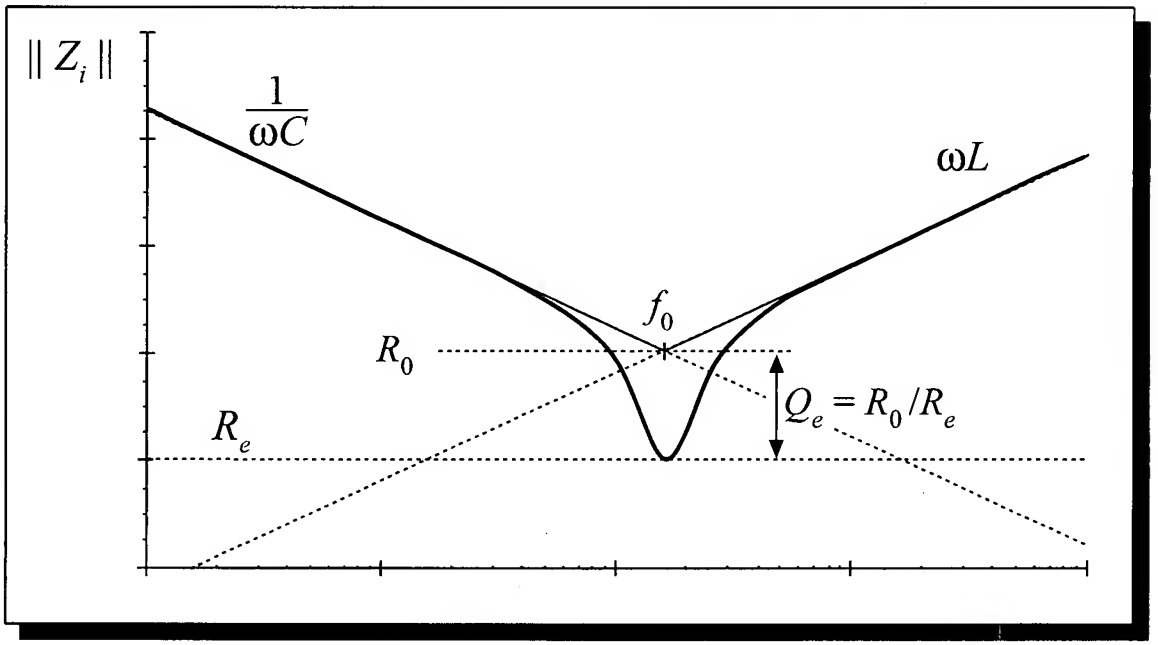
Zero-voltage switching (ZVS) occurs

Tank input impedance

Operation above resonance: tank input impedance Z_i is dominated by tank inductor.

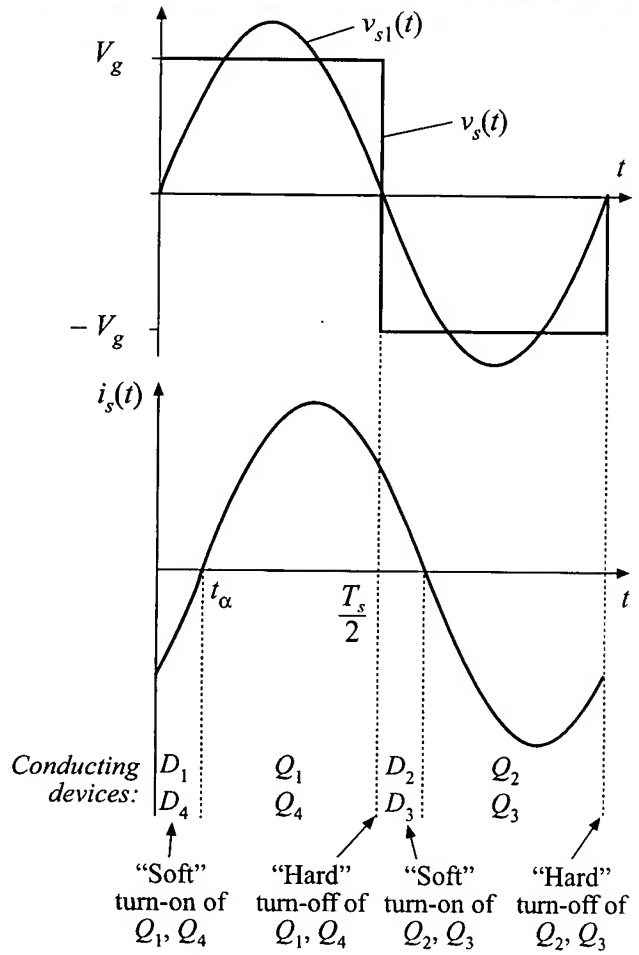
$\angle Z_i$ is negative, and tank input current lags tank input voltage.

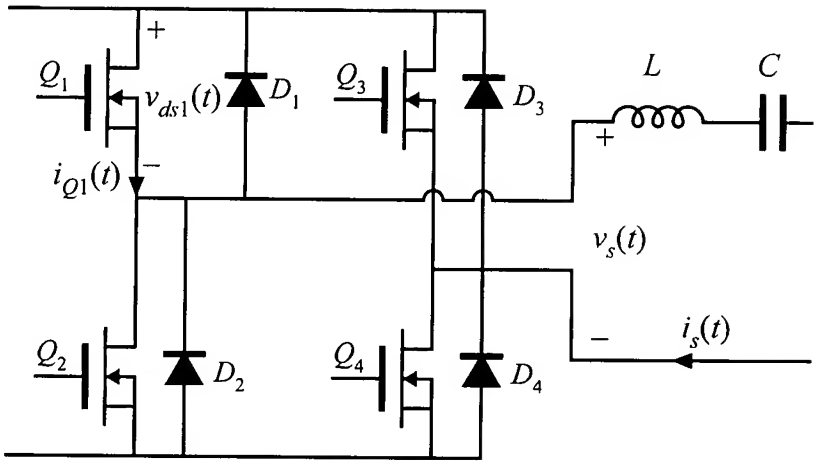
Zero crossing of the tank input current waveform $i_s(t)$ occurs after the zero crossing of the voltage $v_s(t)$.



Switch network waveforms, above resonance

Zero-voltage switching

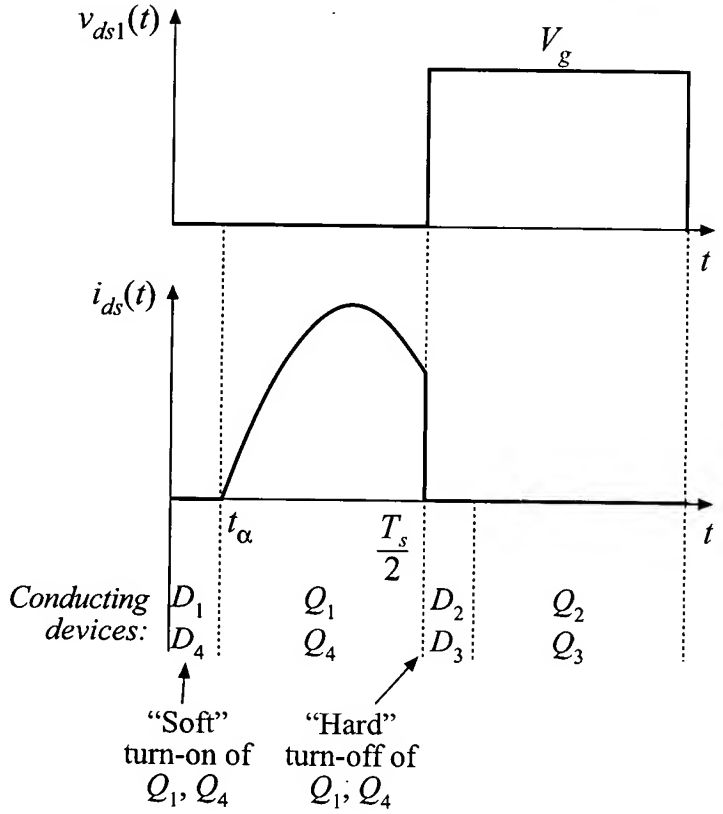


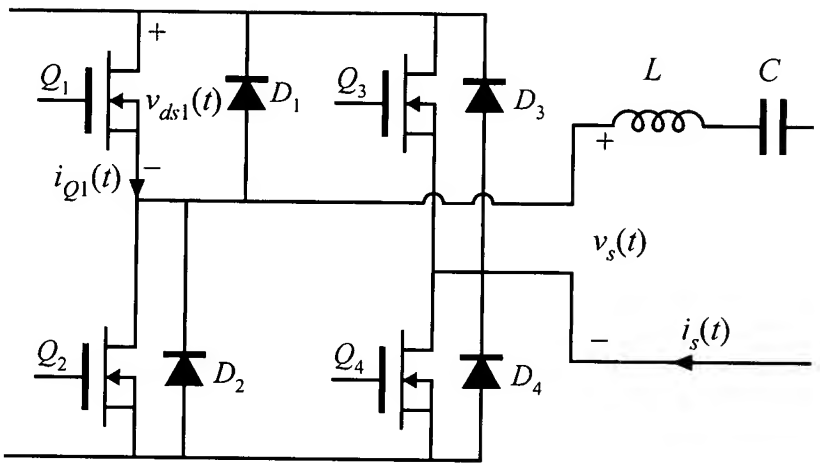


Conduction sequence: D_1–Q_1–D_2–Q_2

Q_1 is turned on during D_1 conduction interval, without loss

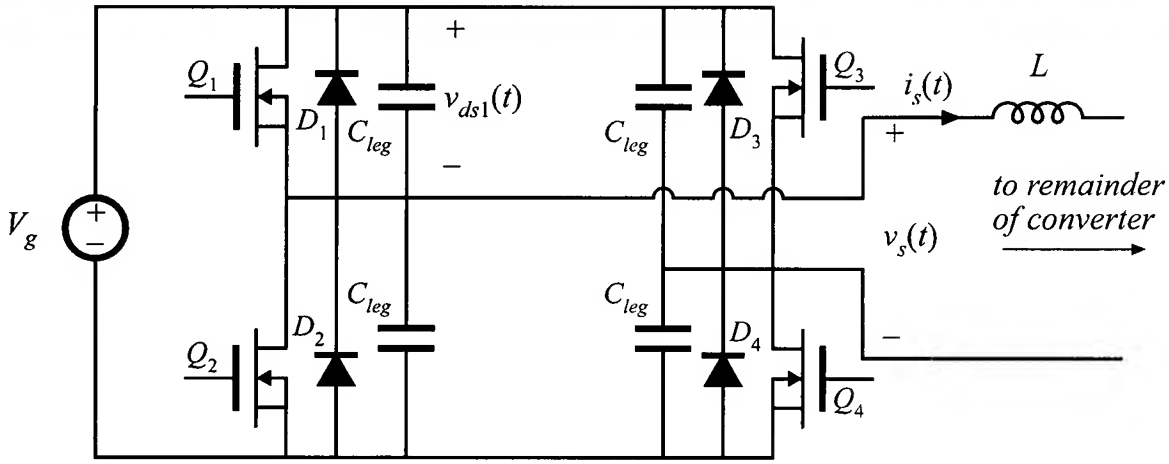
ZVS turn-off transition: hard switching?



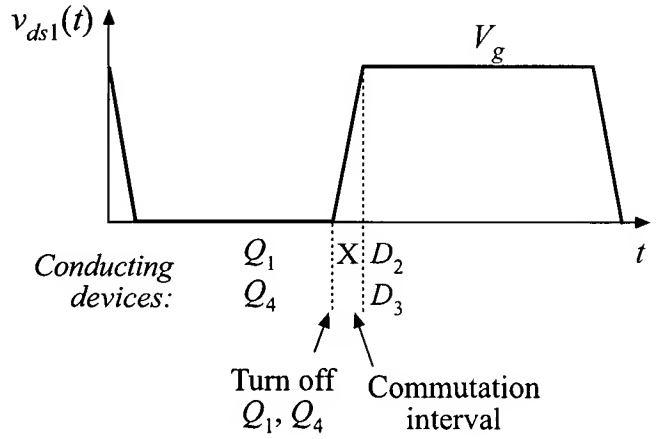


When Q_1 turns off, D_2 must begin conducting. Voltage across Q_1 must increase to V_g. Transistor turn-off transition is identical to hard-switched PWM. Switching loss may occur (but see next slide).

Soft switching at the ZVS turn-off transition



- Introduce small capacitors C_{leg} across each device (or use device output capacitances).
- Introduce delay between turn-off of Q_1 and turn-on of Q_2.

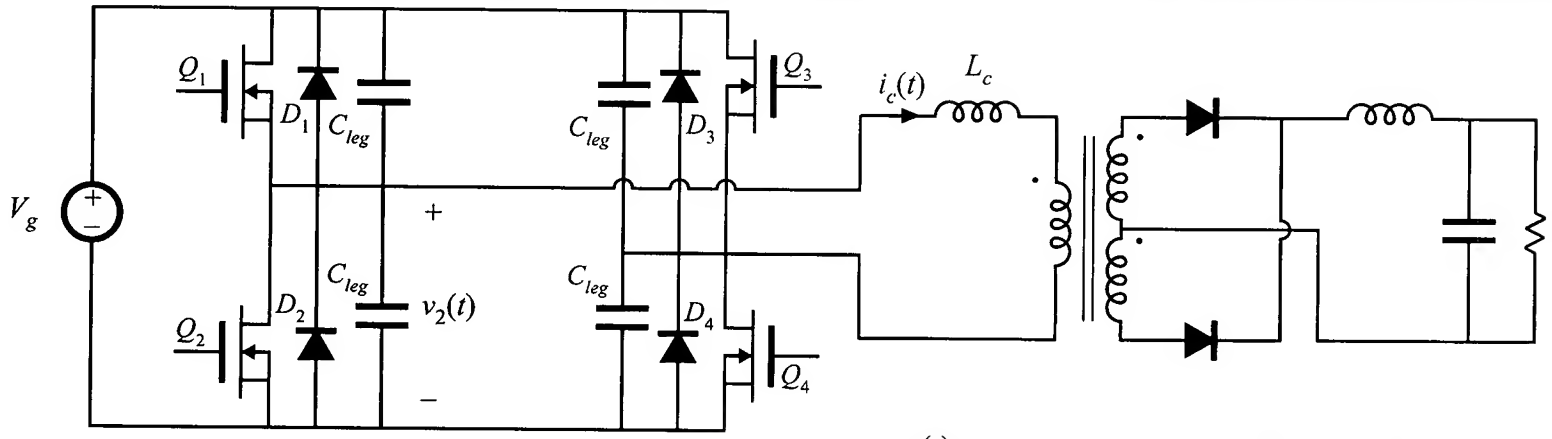


Tank current $i_s(t)$ charges and discharges C_{leg}. Turn-off transition becomes lossless. During commutation interval, no devices conduct.

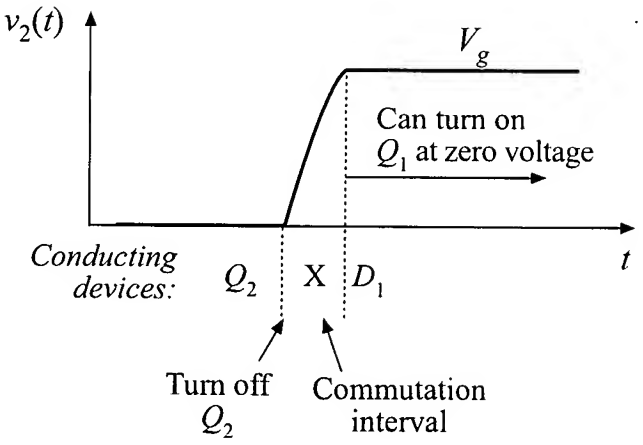
So zero-voltage switching exhibits low switching loss: losses due to diode stored charge and device output capacitances are eliminated.

19.4.3 The zero-voltage transition converter

Basic version based on full-bridge PWM buck converter



- Can obtain ZVS of all primary-side MOSFETs and diodes
- Secondary-side diodes switch at zero-current, with loss
- Phase-shift control



19.5 Load-dependent properties of resonant converters

Resonant inverter design objectives:

1. Operate with a specified load characteristic and range of operating points
   - With a nonlinear load, must properly match inverter output characteristic to load characteristic
2. Obtain zero-voltage switching or zero-current switching
   - Preferably, obtain these properties at all loads
   - Could allow ZVS property to be lost at light load, if necessary
3. Minimize transistor currents and conduction losses
   - To obtain good efficiency at light load, the transistor current should scale proportionally to load current (in resonant converters, it often doesn't!)

Topics of Discussion

Section 19.5

Inverter output i-v characteristics

Two theorems

- Dependence of transistor current on load current
- Dependence of zero-voltage/zero-current switching on load resistance
- Simple, intuitive frequency-domain approach to design of resonant converter

Examples and interpretation

- Series
- Parallel
- LCC

Inverter output characteristics

Let H_∞ be the open-circuit ($R \to \infty$) transfer function:

$$\left.\frac{v_o(j\omega)}{v_i(j\omega)}\right|_{R\to\infty} = H_\infty(j\omega)$$

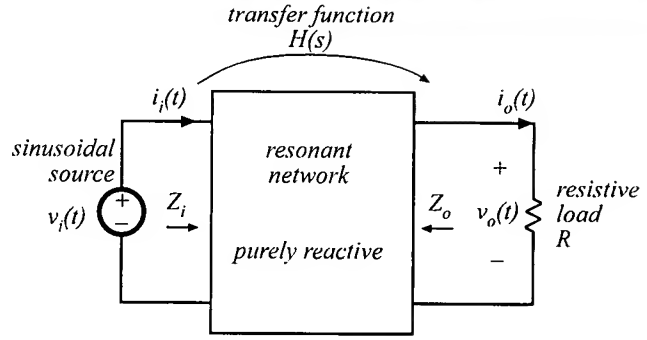
and let Z_{o0} be the output impedance (with $v_i \to$ short-circuit). Then,

$$v_o(j\omega) = H_\infty(j\omega)\, v_i(j\omega)\, \frac{R}{R + Z_{o0}(j\omega)}$$

The output voltage magnitude is:

$$\| v_o \|^2 = v_o v_o^* = \frac{\| H_\infty \|^2 \| v_i \|^2}{\left(1 + \| Z_{o0} \|^2 / R^2\right)}$$

with $\quad R = \| v_o \| / \| i_o \|$



This result can be rearranged to obtain

$$\| v_o \|^2 + \| i_o \|^2 \| Z_{o0} \|^2 = \| H_\infty \|^2 \| v_i \|^2$$

Hence, at a given frequency, the output characteristic (i.e., the relation between $||v_o||$ and $||i_o||$) of any resonant inverter of this class is elliptical.

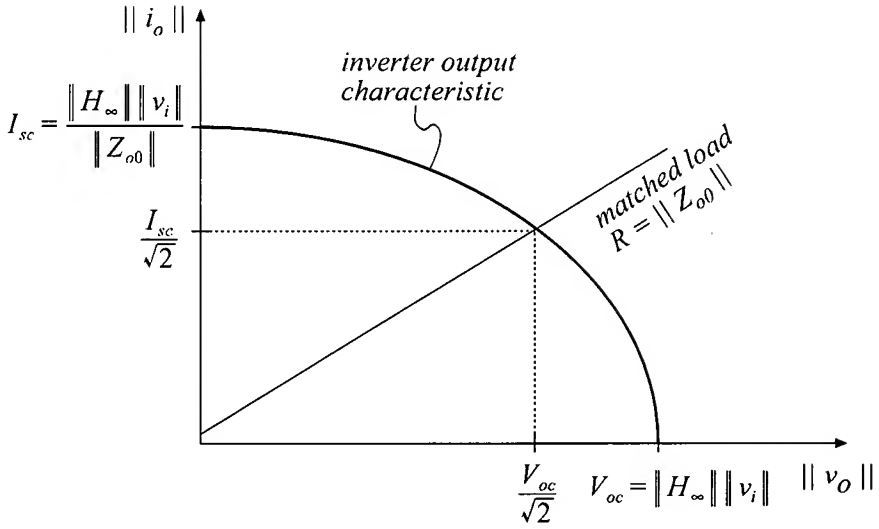
Inverter output characteristics

General resonant inverter output characteristics are elliptical, of the form

$$\frac{\|v_o\|^2}{V_{oc}^2} + \frac{\|i_o\|^2}{I_{sc}^2} = 1$$

with $V_{oc} = \|H_\infty\| \|v_i\|$

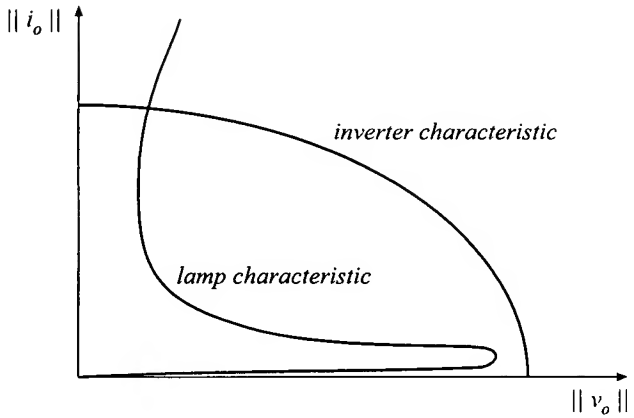
$$I_{sc} = \frac{\|H_\infty\| \|v_i\|}{\|Z_{o0}\|}$$



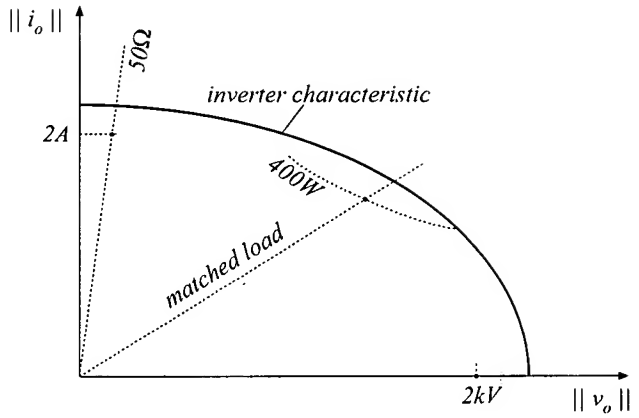
This result is valid provided that *(i)* the resonant network is purely reactive, and *(ii)* the load is purely resistive.

Matching ellipse to application requirements

Electronic ballast

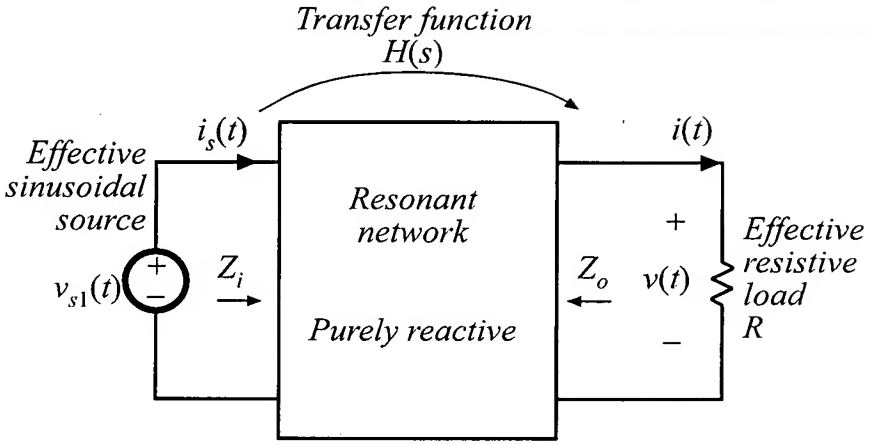


Electrosurgical generator



Input impedance of the resonant tank network

$$Z_i(s) = Z_{i0}(s)\,\frac{1 + \dfrac{R}{Z_{o0}(s)}}{1 + \dfrac{R}{Z_{o\infty}(s)}} = Z_{i\infty}(s)\,\frac{1 + \dfrac{Z_{o0}(s)}{R}}{1 + \dfrac{Z_{o\infty}(s)}{R}}$$



where

$$Z_{i0} = \left.\frac{v_i}{i_i}\right|_{R \to 0} \qquad Z_{i\infty} = \left.\frac{v_i}{i_i}\right|_{R \to \infty} \qquad Z_{o0} = \left.\frac{v_o}{-i_o}\right|_{v_i \to \text{short circuit}} \qquad Z_{o\infty} = \left.\frac{v_o}{-i_o}\right|_{v_i \to \text{open circuit}}$$

Other relations

Reciprocity

$$\frac{Z_{i0}}{Z_{i\infty}} = \frac{Z_{o0}}{Z_{o\infty}}$$

Tank transfer function

$$H(s) = \frac{H_\infty(s)}{1 + \frac{R}{Z_{o0}}}$$

where

$$H_\infty = \left. \frac{\breve{v}_o(s)}{v_i(s)} \right|_{R \to \infty}$$

$$\| H_\infty \|^2 = Z_{o0} \left(\frac{1}{Z_{i0}} - \frac{1}{Z_{i\infty}} \right)$$

If the tank network is purely reactive, then each of its impedances and transfer functions have zero real parts:

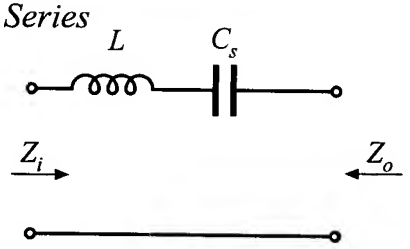
$$Z_{i0} = -Z_{i0}^*$$
$$Z_{i\infty} = -Z_{i\infty}^*$$
$$Z_{o0} = -Z_{o0}^*$$
$$Z_{o\infty} = -Z_{o\infty}^*$$
$$H_\infty = -H_\infty^*$$

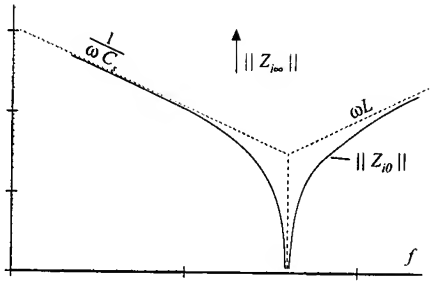
Hence, the input impedance magnitude is

$$\| Z_i \|^2 = Z_i Z_i^* = \| Z_{i0} \|^2 \frac{\left(1 + \frac{R^2}{\| Z_{o0} \|^2} \right)}{\left(1 + \frac{R^2}{\| Z_{o\infty} \|^2} \right)}$$

Z_{i0} and $Z_{i\infty}$ for 3 common inverters

Series

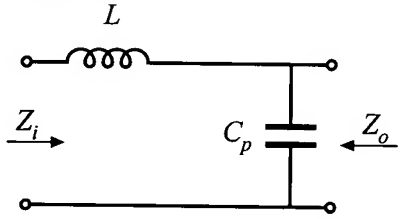


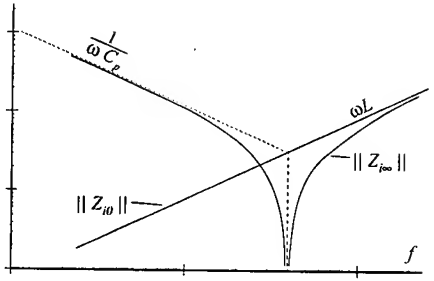


$$Z_{i0}(s) = sL + \frac{1}{sC_s}$$

$$Z_{i\infty}(s) = \infty$$

Parallel

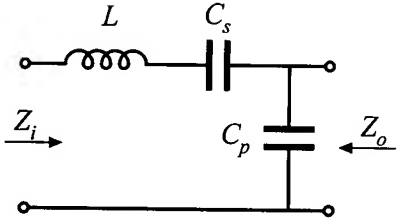


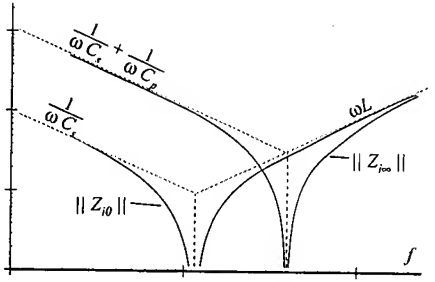


$$Z_{i0}(s) = sL$$

$$Z_{i\infty}(s) = sL + \frac{1}{sC_p}$$

LCC





$$Z_{i0}(s) = sL + \frac{1}{sC_s}$$

$$Z_{i\infty}(s) = sL + \frac{1}{sC_p} + \frac{1}{sC_s}$$

A Theorem relating transistor current variations to load resistance R

Theorem 1: If the tank network is purely reactive, then its input impedance $\| Z_i \|$ is a monotonic function of the load resistance R.

- So as the load resistance R varies from 0 to ∞, the resonant network input impedance $\| Z_i \|$ varies monotonically from the short-circuit value $\| Z_{i0} \|$ to the open-circuit value $\| Z_{i\infty} \|$.
- The impedances $\| Z_{i\infty} \|$ and $\| Z_{i0} \|$ are easy to construct.
- If you want to minimize the circulating tank currents at light load, maximize $\| Z_{i\infty} \|$.
- Note: for many inverters, $\| Z_{i\infty} \| < \| Z_{i0} \|$! The no-load transistor current is therefore greater than the short-circuit transistor current.

Proof of Theorem 1

Previously shown:

$$\| Z_i \|^2 = \| Z_{i0} \|^2 \frac{\left(1 + \frac{R}{\| Z_{o0} \|^2} \right)}{\left(1 + \frac{R}{\| Z_{o\infty} \|^2} \right)}$$

➡ Differentiate:

$$\frac{d \| Z_i \|^2}{d R} = 2 \| Z_{i0} \|^2 \frac{\left(\frac{1}{\| Z_{o0} \|^2} - \frac{1}{\| Z_{o\infty} \|^2} \right) R}{\left(1 + \frac{R^2}{\| Z_{o\infty} \|^2} \right)^2}$$

➡ Derivative has roots at:

(*i*) $R = 0$

(*ii*) $R = \infty$

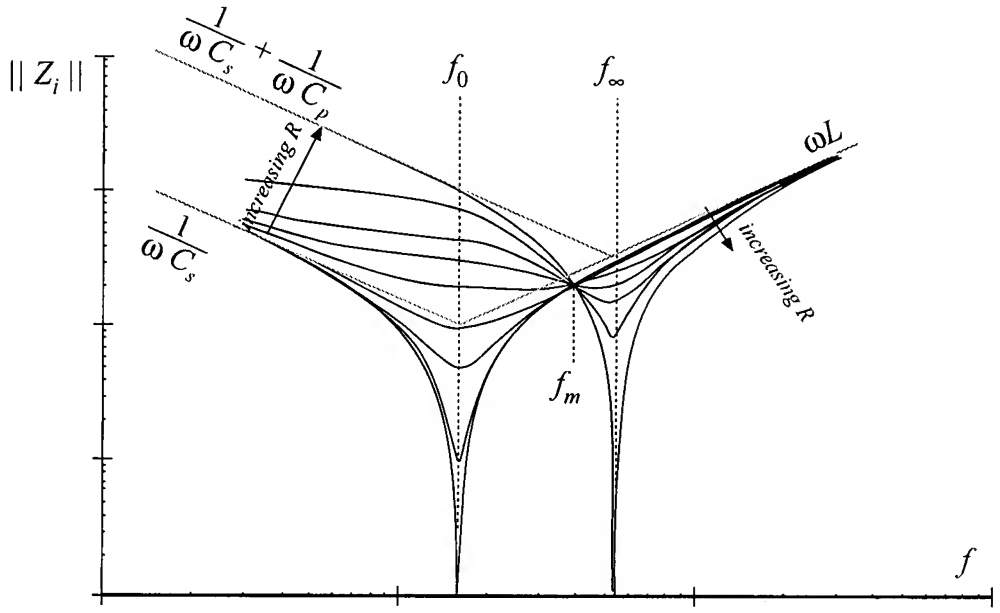
(*iii*) $\| Z_{o0} \| = \| Z_{o\infty} \|$, *or* $\| Z_{i0} \| = \| Z_{i\infty} \|$

So the resonant network input impedance is a monotonic function of R, over the range 0 < R < ∞.

In the special case $\| Z_{i0} \| = \| Z_{i\infty} \|$, $\| Z_i \|$ is independent of R.

Example: $||Z_i||$ of LCC

- for $f < f_m$, $||Z_i||$ increases with increasing R.
- for $f > f_m$, $||Z_i||$ decreases with increasing R.
- at a given frequency f, $||Z_i||$ is a monotonic function of R.
- It's not necessary to draw the entire plot: just construct $||Z_{i0}||$ and $||Z_{i\infty}||$.



Discussion: LCC

$\| Z_{i0} \|$ and $\| Z_{i\infty} \|$ both represent series resonant impedances, whose Bode diagrams are easily constructed.

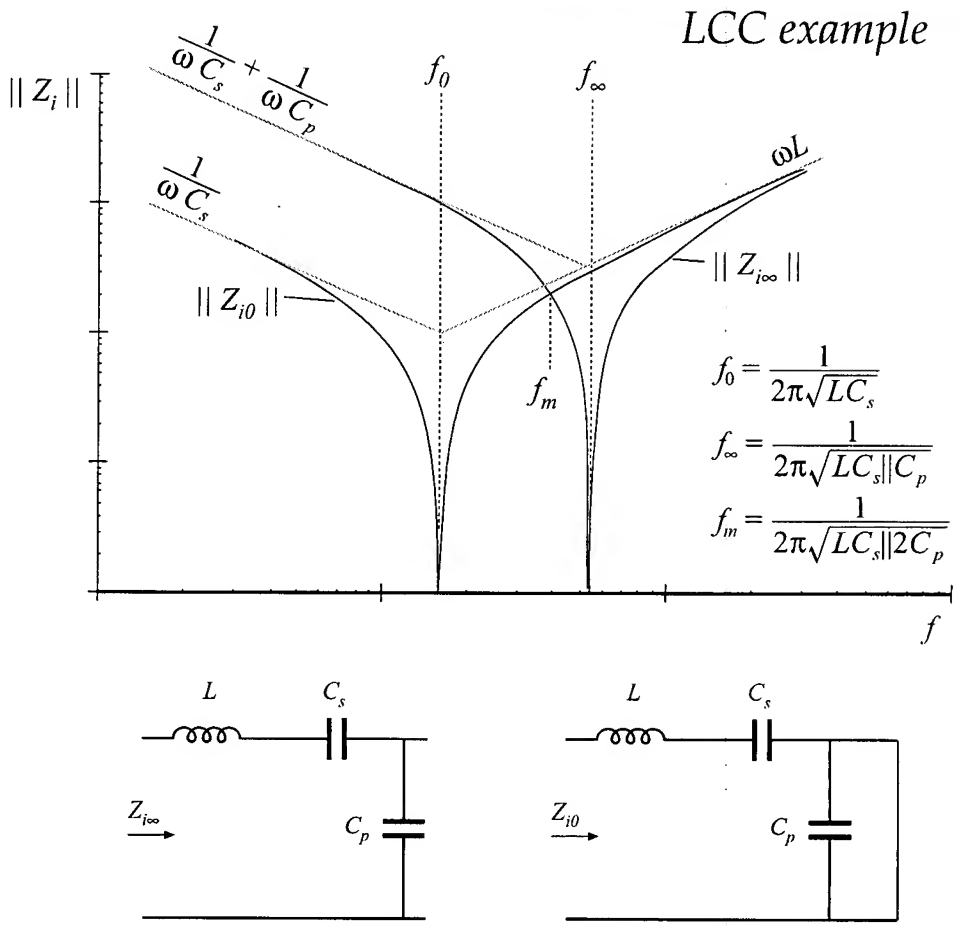
$\| Z_{i0} \|$ and $\| Z_{i\infty} \|$ intersect at frequency f_m.

For $f < f_m$

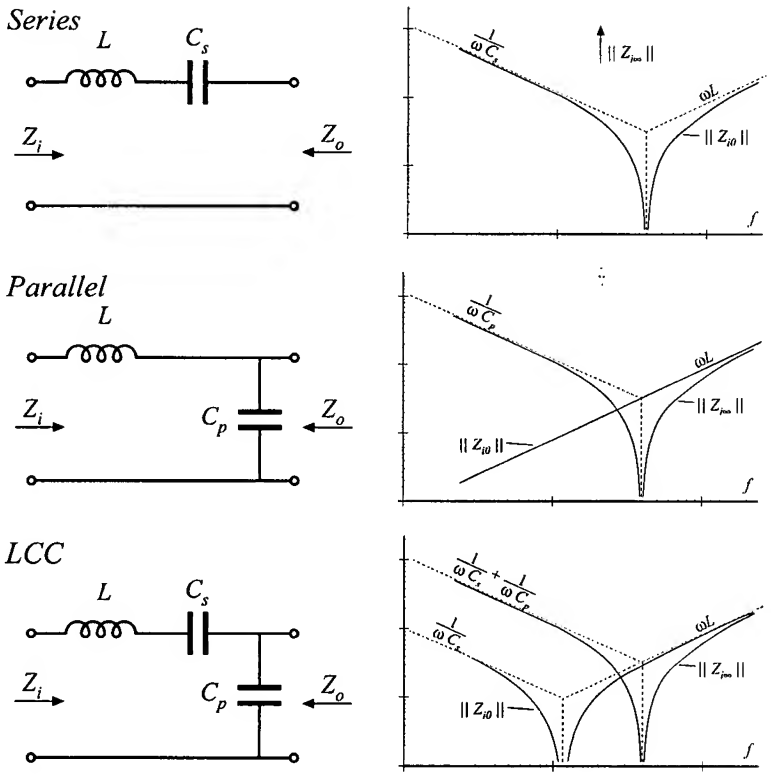
then $\| Z_{i0} \| < \| Z_{i\infty} \|$; hence transistor current decreases as load current decreases

For $f > f_m$

then $\| Z_{i0} \| > \| Z_{i\infty} \|$; hence transistor current increases as load current decreases, and transistor current is greater than or equal to short-circuit current for all R



Discussion -series and parallel



- No-load transistor current = 0, both above and below resonance.
- ZCS below resonance, ZVS above resonance
- Above resonance: no-load transistor current is *greater* than short-circuit transistor current. ZVS.
- Below resonance: no-load transistor current is less than short-circuit current (for $f < f_m$), but determined by $\| Z_{i\infty} \|$. ZCS.

A Theorem relating the ZVS/ZCS boundary to load resistance R

Theorem 2: If the tank network is purely reactive, then the boundary between zero-current switching and zero-voltage switching occurs when the load resistance R is equal to the critical value R_{crit}, given by

$$R_{crit} = \| Z_{o0} \| \sqrt{\frac{-Z_{i\infty}}{Z_{i0}}}$$

It is assumed that zero-current switching (ZCS) occurs when the tank input impedance is capacitive in nature, while zero-voltage switching (ZVS) occurs when the tank is inductive in nature. This assumption gives a necessary but not sufficient condition for ZVS when significant semiconductor output capacitance is present.

Proof of Theorem 2

Previously shown:

$$Z_i = Z_{i\infty} \frac{1 + \frac{Z_{o0}}{R}}{1 + \frac{Z_{o\infty}}{R}}$$

If ZCS occurs when Z_i is capacitive, while ZVS occurs when Z_i is inductive, then the boundary is determined by $\angle Z_i = 0$. Hence, the critical load R_{crit} is the resistance which causes the imaginary part of Z_i to be zero:

$$\mathrm{Im}\left(Z_i(R_{crit})\right) = 0$$

Note that $Z_{i\infty}$, Z_{o0}, and $Z_{o\infty}$ have zero real parts. Hence,

$$\mathrm{Im}\left(Z_i(R_{crit})\right) = \mathrm{Im}\left(Z_{i\infty}\right) \mathrm{Re}\left(\frac{1 + \frac{Z_{o0}}{R_{crit}}}{1 + \frac{Z_{o\infty}}{R_{crit}}}\right)$$

$$= \mathrm{Im}\left(Z_{i\infty}\right) \mathrm{Re}\left(\frac{1 - \frac{Z_{o0}Z_{o\infty}}{R_{crit}^2}}{1 + \frac{\|Z_{o\infty}\|^2}{R_{crit}^2}}\right)$$

Solution for R_{crit} yields

$$R_{crit} = \|Z_{o0}\| \sqrt{\frac{-Z_{i\infty}}{Z_{i0}}}$$

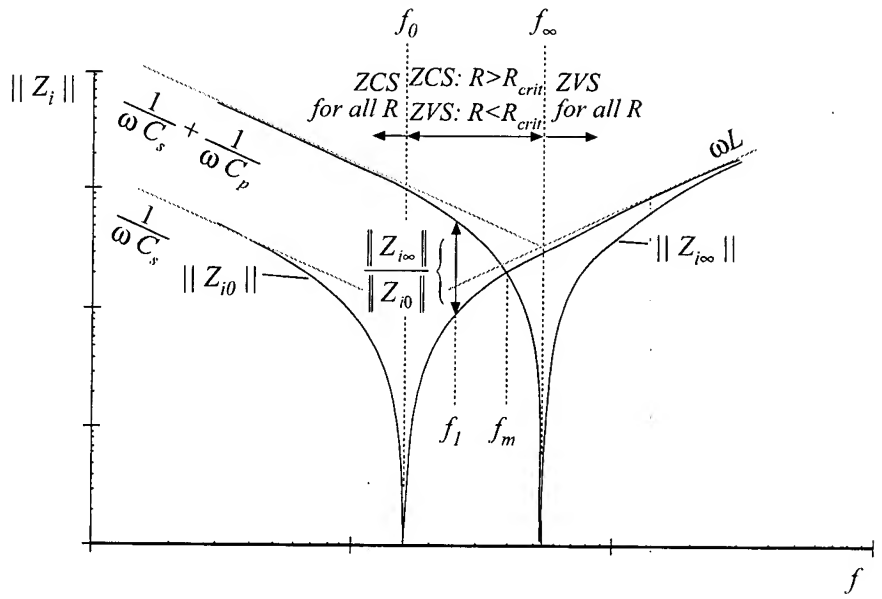
Discussion —Theorem 2

$$R_{crit} = \| Z_{o0} \| \sqrt{\frac{-Z_{i\infty}}{Z_{i0}}}$$

- Again, $Z_{i\infty}$, Z_{i0}, and Z_{o0} are pure imaginary quantities.
- If $Z_{i\infty}$ and Z_{i0} have the same phase (both inductive or both capacitive), then there is no real solution for R_{crit}.
- Hence, if at a given frequency $Z_{i\infty}$ and Z_{i0} are both capacitive, then ZCS occurs for all loads. If $Z_{i\infty}$ and Z_{i0} are both inductive, then ZVS occurs for all loads.
- If $Z_{i\infty}$ and Z_{i0} have opposite phase (one is capacitive and the other is inductive), then there is a real solution for R_{crit}. The boundary between ZVS and ZCS operation is then given by $R = R_{crit}$.
- Note that $R = \| Z_{o0} \|$ corresponds to operation at matched load with maximum output power. The boundary is expressed in terms of this matched load impedance, and the ratio $Z_{i\infty} / Z_{i0}$.

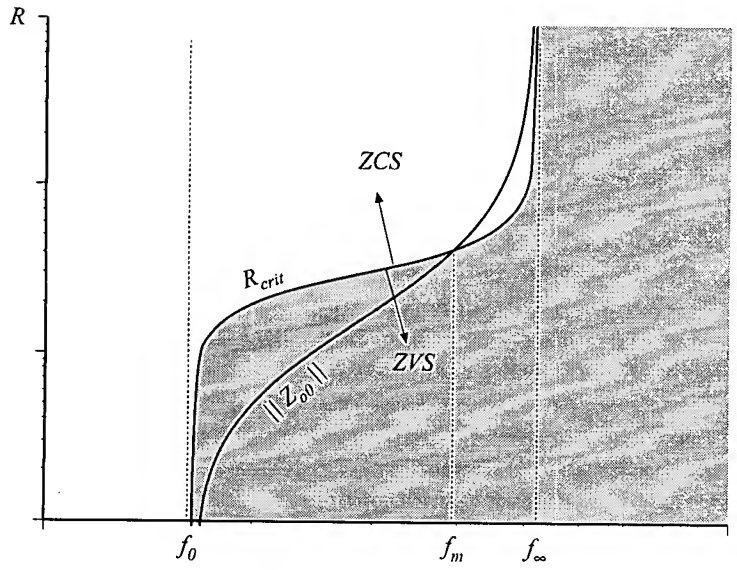
LCC example

- For $f > f_\infty$, ZVS occurs for all R.
- For $f < f_0$, ZCS occurs for all R.
- For $f_0 < f < f_\infty$, ZVS occurs for $R < R_{crit}$, and ZCS occurs for $R > R_{crit}$.
- Note that $R = \| Z_{o0} \|$ corresponds to operation at matched load with maximum output power. The boundary is expressed in terms of this matched load impedance, and the ratio $Z_{i\infty} / Z_{i0}$.

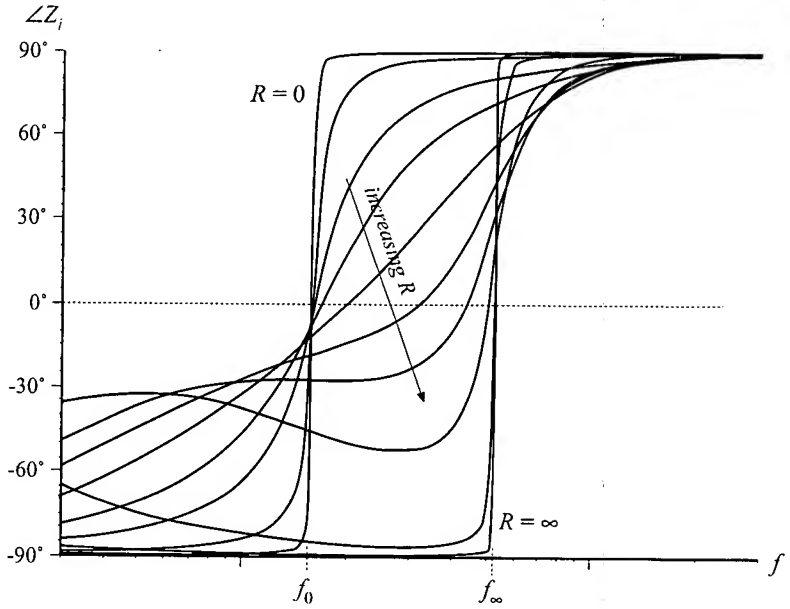


$$R_{crit} = \| Z_{o0} \| \sqrt{\frac{-Z_{i\infty}}{Z_{i0}}}$$

LCC example, continued



Typical dependence of R_{crit} and matched-load impedance $||Z_{o0}||$ on frequency f, LCC example.



Typical dependence of tank input impedance phase vs. load R and frequency, LCC example.

19.6 Summary of Key Points

1. The sinusoidal approximation allows a great deal of insight to be gained into the operation of resonant inverters and dc–dc converters. The voltage conversion ratio of dc–dc resonant converters can be directly related to the tank network transfer function. Other important converter properties, such as the output characteristics, dependence (or lack thereof) of transistor current on load current, and zero-voltage- and zero-current-switching transitions, can also be understood using this approximation. The approximation is accurate provided that the effective Q–factor is sufficiently large, and provided that the switching frequency is sufficiently close to resonance.
2. Simple equivalent circuits are derived, which represent the fundamental components of the tank network waveforms, and the dc components of the dc terminal waveforms.

Summary of key points

3. Exact solutions of the ideal dc–dc series and parallel resonant converters are listed here as well. These solutions correctly predict the conversion ratios, for operation not only in the fundamental continuous conduction mode, but in discontinuous and subharmonic modes as well.
4. Zero-voltage switching mitigates the switching loss caused by diode recovered charge and semiconductor device output capacitances. When the objective is to minimize switching loss and EMI, it is preferable to operate each MOSFET and diode with zero-voltage switching.
5. Zero-current switching leads to natural commutation of SCRs, and can also mitigate the switching loss due to current tailing in IGBTs.

Summary of key points

6. The input impedance magnitude $\| Z_i \|$, and hence also the transistor current magnitude, are monotonic functions of the load resistance R. The dependence of the transistor conduction loss on the load current can be easily understood by simply plotting $\| Z_i \|$ in the limiting cases as $R \to \infty$ and as $R \to 0$, or $\| Z_{i\infty} \|$ and $\| Z_{i0} \|$.
7. The ZVS/ZCS boundary is also a simple function of $Z_{i\infty}$ and Z_{i0}. If ZVS occurs at open-circuit and at short-circuit, then ZVS occurs for all loads. If ZVS occurs at short-circuit, and ZCS occurs at open-circuit, then ZVS is obtained at matched load provided that $\| Z_{i\infty} \| > \| Z_{i0} \|$.
8. The output characteristics of all resonant inverters considered here are elliptical, and are described completely by the open-circuit transfer function magnitude $\| H_\infty \|$, and the output impedance $\| Z_{o0} \|$. These quantities can be chosen to match the output characteristics to the application requirements.